Deliverable D3.2 Atomic defect properties from the electrical measurements on GeSe OTS selectors





D3.2

Atomic defect properties from the electrical measurements on GeSe OTS selectors

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Executive Summary

This document provides a description of the use of the device cycle of the IM2D Simulation box to extract material and defect properties from the interpretation of the electrical current-voltage (I-V) characteristics measured on Ovonic Threshold Switching (OTS) selector devices. It is developed within Work Package 3, "Testing and piloting", and its task n. 3.3, "Task 3.3. From OTS selector electrical characteristics to key material/defect properties", with AMAT as task leader and contributions from CNR, ICN2, AMAT, FMC, IMEC.

The task activities rely on the use of the Defect Discovery Tool (DDT) functionalities implemented into AMAT proprietary GinestraTM platform, that are specifically developed to extract intrinsic material/device properties (bandgap, thicknesses) and characteristics of the defects (thermal ionization and relaxation energies, distribution within the bandgap) from electrical measurements. Further details on DDT can be found in Sec 3.2 of Deliverable 3.1.

DDT functionalities are applied to current-voltage and conductance-voltage (G-V) characteristics measured on GeSe-based OTS devices with different thicknesses (10nm and 20nm) and compositions ($Ge_{60}Se_{40}$ and $Ge_{50}Se_{50}$). Capacitance-Voltage characteristics (C-V) are used to provide an estimation of the relative dielectric permittivity of the GeSe film. All devices and electrical measurements are provided by the IMEC unit.

Consistent results are obtained for all the considered samples. Derived material parameters (band-gap and relative dielectric permittivity) well agree with reports in literature and with the Density Functional Theory (DFT) calculations performed within the project and presented in this Deliverable. An increase of GeSe band-gap is observed as the Ge content of the film is reduced (from $Ge_{60}Se_{40}$ to $Ge_{50}Se_{50}$).

The experimental I-V characteristics and their temperature dependence are well explained by a trap-assisted carrier transport, occurring through a defect-band located close to the GeSe valence band minima. The traps energy levels (within the band-gap) extracted with the DDT functionalities are found to be in good agreement with the values reported in Selenium vacancies (V_{Se}) literature. However, a precise identification of the defect atomic structure is not straightforward, since the value of the relaxation energy cannot be unambiguously identified.

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1. Introduction

One of the goals behind the INTERSECT project is to setup an Interoperable Materials to device framework able to integrate materials modelling codes in a way that allows mutual interaction and exchange of information. In order to test the IM2D simulation box infrastructure, AMAT and the other project partners identified two pilot cases to be used for piloting and testing.

This report focuses on the pilot case for the development of solutions for OTS materials for selector applications. More specifically, it addresses the device-to-material workflow that is the extraction of defects properties from electrical measurements. On one hand, the main physical aspects related to this piloting problem will constitute the input for the formalization of use cases, and their translation into interoperable workflows will be done in WP1 and implemented in WP2. On the other hand, calculations will be performed using the beta versions of the code that are implemented in WP1-2 during the project.

This document describes the status of Deliverable D3.2, concerning the application of the IM2D toolbox to the pilot case of OTS selector devices.

2. Extraction of OTS atomic defect properties

2.1 Devices and Experimental Data

In total, six different Ge_xSe_{1-x} OTS layer combinations were selected and studied in this project, with layer thicknesses 10 and 20 nm and Ge concentration x ranging from ~40% to 60% (IMEC lots AL704260 and AL8043354/1, cf. Table I).

The amorphous GeSe films were prepared by room temperature physical vapor deposition (PVD). The layers were integrated into TiN/GeSe/TiN two-terminal structures in a 300 mm process flow and passivated with a low-temperature -Back End Of Line (BEOL) process [1]. Carbon top electrode was applied for one case (AL8043354/1D23, Table I) to reduce leakage.

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Table I – Ge_xSe_{1-x} layers studied in this project, comprising two splits with 10 nm GeSe with varying Ge content and four splitswith 20 nm OTS with varying Ge content and varying top electrode.

Sample ID	Wafer (split)	M \ I \ M
D12	AL704260D12	TiN \ 10 nm $Ge_{41}Se_{59}$ \ TiN
D16	AL704260D16	TiN \ 10 nm Ge ₆₀ Se₄0 \ TiN
D20	AL8043354/1D20	TiN ∖ 20 nm Ge₄₄Se₅ ∖ TiN
D21	AL8043354/1D21	TiN ∖ 20 nm Ge₅₀Se₅₀ ∖ TiN
D22	AL8043354/1D22	TiN ∖ 20 nm Ge ₆₀ Se ₄₀ ∖ TiN
D23	AL8043354/1D23	TiN \ 20 nm Ge ₆₀ Se₄₀ \ 6 nm C \ TiN

Each 300 mm wafer was divided into 151 dies, each of which was patterned with IMEC "TANGO" mask-set containing modules with two-terminal Metal Insulator Metal (MIM) devices measured in this project. Two types of structures were used, namely square RREL with varying area (Fig. 1, Table II) and high-perimeter comb-like RPERI, with constant area and varying perimeter (Fig. 2, Table III).



Figure 1 – The RREL module with square devices (between top and bottom electrodes) with varying areas.

Table II – In total, eight RREL modules n = 01 through 08 were fabricated on each die. Square devices 7 through 12, with varying areas (width*height) were used.

RREL <i>n</i> _	Area (um ²)
7	30*30
8	10*10
9	3*3
10	1*1
11	0.3*0.3
12	0.1*0.1



Figure 2 – An example of the high-perimeter comb-like RPERI structure. Three fingers are visible.

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RPERI <i>n</i> _	Finger width (um)	Finger length (um)	Finger number ()	Equivalent area (um ²)
12	10	10	1	10*10
11	10	5	2	10*10
10	10	3.33	3	10*10
9	10	2.5	4	10*10
8	10	1.25	8	10*10
7	10	0.625	16	10*10
6	10	0.3	33	10*10
5	10	0.15	67	10*10
4	10	0.1	100	10*10
3	10	0.08	125	10*10
2	10	0.065	154	10*10
1	10	0.045	222	10*10

 Table III – In total, four RPERI modules n = 01 through 04 were fabricated on each die. Devices 1 through 12, with varying number of fingers, and hence varying perimeters, but fixed total area, were used.

Positions (x, y) of all dies and measured structures were described (Fig. 3) to enable automation of the entire measurement (prober and measuring instruments).

<pre>test_chip => 2 , x => -25605 , y => -15260 test_chip => 3 , x => 0 , y => -15260 test_chip => 4 , x => 25605 , y => -15260 test_chip => 4 , x => 25605 , y => -15260 test_chip => 5 , x => 51210 , y => -15260 test_device => RREL01_3 , x => -17910 , y => 200 test_chip => 6 , x => 76815 , y => -15260 test_device => RREL01_4 , x => -17910 , y => 300 test_chip => 7 , x => -51210 , y => -15260 test_device => RREL01_6 , x => -17910 , y => 400 test_chip => 8 , x => -25605 , y => -30520 test_device => RREL01_7 , x => -17910 , y => 600 test_chip => 9 , x => 0 , y => -30520 test_device => RREL01_9 , x => -17910 , y => 800 test_chip => 10 , x => 25605 , y => -30520 test_device => RREL01_9 , x => -17910 , y => 900 test_chip => 11 , x => 51210 , y => -30520 test_device => RREL01_11 , x => -17910 , y => 1000 test_chip => 12 , x => 76815 , y => -30520 test_device => RREL01_12 , x => -17910 , y => 1000 test_device => RREL01_12 , x => -17910 , y => 1000 test_device => RREL01_11 , x => -17910 , y => 1000 test_device => RREL01_12 , x => -17910 , y => 1000</pre>	test chip	=>	1	,	х	=>	25605	,	у	=>	0	test_device	=>	RREL01_1	,	х	=>	-17910	,	У	=>	0
<pre>test_chip => 3 , x => 0 , y => -15260 test_device => RREL01_3 , x => -17910 , y => 200 test_chip => 4 , x => 25605 , y => -15260 test_device => RREL01_4 , x => -17910 , y => 300 test_chip => 5 , x => 51210 , y => -15260 test_device => RREL01_5 , x => -17910 , y => 300 test_chip => 6 , x => 76815 , y => -15260 test_device => RREL01_5 , x => -17910 , y => 400 test_chip => 7 , x => -51210 , y => -30520 test_device => RREL01_7 , x => -17910 , y => 500 test_chip => 8 , x => -25605 , y => -30520 test_device => RREL01_8 , x => -17910 , y => 600 test_chip => 9 , x => 0 , y => -30520 test_device => RREL01_8 , x => -17910 , y => 700 test_chip => 10 , x => 25605 , y => -30520 test_device => RREL01_9 , x => -17910 , y => 900 test_chip => 11 , x => 51210 , y => -30520 test_device => RREL01_11 , x => -17910 , y => 1000 test_chip => 12 , x => 76815 , y => -30520 test_device => RREL01_12 , x => -17910 , y => 1100</pre>	test chip	=>	2	,	х	=>	-25605	,	У	=>	-15260	test_device	=>	RREL01_2	,	х	=>	-17910	,	У	=>	100
<pre>test_chip => 4 , x => 25605 , y => -15260 test_device => RREL01_4 , x => -17910 , y => 300 test_chip => 5 , x => 51210 , y => -15260 test_device => RREL01_5 , x => -17910 , y => 400 test_chip => 6 , x => 76815 , y => -15260 test_device => RREL01_6 , x => -17910 , y => 400 test_chip => 7 , x => -51210 , y => -30520 test_device => RREL01_7 , x => -17910 , y => 500 test_chip => 8 , x => -25605 , y => -30520 test_device => RREL01_8 , x => -17910 , y => 600 test_chip => 9 , x => 0 , y => -30520 test_device => RREL01_9 , x => -17910 , y => 600 test_chip => 10 , x => 25605 , y => -30520 test_device => RREL01_9 , x => -17910 , y => 800 test_chip => 11 , x => 51210 , y => -30520 test_device => RREL01_10 , x => -17910 , y => 900 test_chip => 12 , x => 76815 , y => -30520 test_device => RREL01_11 , x => -17910 , y => 1000 test_device => RREL01_12 , x => -17910 , y => 1100</pre>	test chip	=>	3	,	х	=>	0	,	У	=>	-15260	test_device	=>	RREL01_3	,	х	=>	-17910	,	У	=>	200
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test chip	=>	4	,	х	=>	25605	,	У	=>	-15260	test_device	=>	RREL01_4	,	х	=>	-17910	,	У	=>	300
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test chip	=>	5	,	х	=>	51210	,	У	=>	-15260	test_device	=>	RREL01_5	,	х	=>	-17910	,	У	=>	400
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test_chip	=>	6	,	х	=>	76815	,	У	=>	-15260	test_device	=>	RREL01_6	,	х	=>	-17910	,	У	=>	500
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test_chip	=>	7	,	х	=>	-51210	,	У	=>	-30520	test_device	=>	RREL01_7	,	х	=>	-17910	,	У	=>	600
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test_chip	=>	8	,	х	=>	-25605	,	У	=>	-30520	test_device	=>	RREL01_8	,	х	=>	-17910	,	У	=>	700
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	test_chip	=>	9	,	х	=>	0	,	У	=>	-30520	test_device	=>	RREL01_9	,	х	=>	-17910	,	У	=>	800
$ test_chip => 11 , x => 51210 , y => -30520 \\ test_chip => 12 , x => 76815 , y => -30520 \\ test_device => RREL01_11 , x => -17910 , y => 1000 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 , y => 1100 \\ test_device => RREL01_12 , x => -17910 \\ $	test_chip	=>	10	,	х	=>	25605	,	У	=>	-30520	test_device	=>	RREL01_10	,	х	=>	-17910	,	У	=>	900
$\texttt{test_chip} \implies 12 \mbox{, } x \implies 76815 \mbox{, } y \implies -30520 \qquad \texttt{test_device} \implies \texttt{RREL01_12} \mbox{, } x \implies -17910 \mbox{, } y \implies 1100$	test_chip	=>	11	,	х	=>	51210	,	У	=>	-30520	test_device	=>	RREL01_11	,	х	=>	-17910	,	У	=>	1000
	test_chip	=>	12	,	х	=>	76815	,	У	=>	-30520	test_device	=>	RREL01_12	,	х	=>	-17910	,	У	=>	1100

Figure 3 – Illustration of (left) die (test chip) and (right) measured structure (test device) description of x, y positions on the wafer.

I-V and C/G-V-f measurements were carried at varying temperatures with the following parameters:I-V:

- Keithley 2536 SMU
- V swept from 0 to -2 V (or -5 V) or from 0 to +2 V (or +5V, depending on observed current)
- T = 25 125 oC
- Devices with widely varying areas and measured perimeters

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C/G-V-f:

- Agilent E4980A LCR
- V range +-2 V, in a "safely increasing" pattern 0V, 0.2V, -0.2V, 0.4V, -0.4V, 0.6V, -0.6V, ...
- f range 20 Hz 2 MHz (log distributed) at each V
- Small signal Vac = 30 mV
- CPG model enabled
- T = 25 125 oC
- Devices with two largest (square) areas measured (30*30 and 10*10 um2) to obtain sufficient signal

Each (I-V or C/G-V-f) measurement was performed on a fresh device, and multiple (at least 3) same-sized devices were measured at each measurement condition. Results were afterwards overlaid to identify typical behavior, and the outliers were manually censored out.

On sample D12 (TiN\10nmGe₄₁Se₅₉\TiN), I-V and C/G-V-f measurements were performed only at 25°C, as no reproducible data could be obtained (not shown). Better reproducibility has been obtained on the other 10 nm GeSe sample TiN\10nmGe₆₀Se₄₀\TiN (D16). However, due to the relatively high leakage (Fig. 4), which strongly affects the C/G-V-f measurements (Fig. 5), the measurements were limited to two temperatures. From Figure 4, it is also apparent that current densities measured on RREL and RPERI structures do not fully match. In such cases, measurements on low-perimeter RREL structures should be used over measurement from high-perimeter RPERI structures.



Figure 4 – Leakage current measured as a function of the temperature on $TiN\10nmGe_{60}Se_{40}\TiN$ (D16).



Figure 5 – TiN\10nmGe₆₀Se₄₀\TiN (D16) C-V-f and G-V-f vs T

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Lower leakage was generally achieved on the 20 nm SeGe samples. Reproducible measurements on sample TiN\20nmGe₄₄Se₅₆\TiN (D20) could not be achieved, even though hundreds of devices were tested (not shown). However, on the other three samples from this lot, measurements were reproducible (Figs. 6-10). On samples TiN\20nmGe₆₀Se₄₀\TiN (D22) and TiN\20nmGe₆₀Se₄₀\6nmC\TiN (D23), the I-V curves taken RREL structures did not perfectly scale with those taken on the RPERI structures again, probably due extra perimeter leakage. Hence, only I-V curves from RREL structures were used.



Figure 6 – Leakage current measured as a function of the temperature on $TiN\20nmGe_{50}Se_{50}\TiN$ (D21) in the (left) +-2V and (right) +-5V ranges.



Figure 7 – TiN 20nm $Ge_{50}Se_{50}$ TiN (D21) C-V-f and G-V-f vs T.

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Figure 8 – Leakage current measured as a function of the temperature on (left) $TiN\20nmGe_{60}Se_{40}\TiN$ (D22) and $TiN\20nmGe_{60}Se_{40}\TiN$ (D23) samples.



Figure 9 – TiN\20nmGe60Se40\TiN (D22) C-V-f and G-V-f vs T.

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Figure 10 - TiN\20nmGe60Se40\6nmC\TiN (D23) C-V-f and G-V-f vs T.

2.2 The Defect Discovery Tool (DDT)

The experimental data provided by IMEC unit are fed into the Ginestra[™] DDT. DDT is a unique functionality of Ginestra[™], specifically developed with the aim of reproducing the voltage, frequency and temperature dependence of I-V and G-V characteristics, in order to extract relevant material parameters and trap energy/space distribution. Figure 11 shows a schematic representation of the DDT workflow for the case of the leakage current measured on a single-layer MIM capacitor. It is comprised of four main steps:

- 1. Measured device/structure is re-created within the Ginestra[™] simulation platform, starting from the known device and material parameters (layers thickness, band-gap, dielectric constant, etc.).
- 2. Measured experimental data are loaded into the DDT the gate leakage currents as a function of the temperature shown on the left side of Figure 11.
- Device, material and more importantly trap parameters to be extracted (as well as their variation ranges) are selected from a dedicated panel of the DDT, see the central part of Figure 11.
- 4. After DDT run, the selected parameters will be automatically varied within the specified intervals until the experimental data are accurately reproduced, see the right part of Figure 11. This process allows to extract the energy and space distribution of the traps as part of the final results.



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Figure 11 - schematic representation of the DDT workflow for the case of the leakage current measured on a single-layer MIM capacitor.

2.3 Results and Discussion

The DDT-based methodology described in the previous section is applied to the GeSe samples described in Section 3.1.

As a preliminary step, we used the C-V data to estimate the relative dielectric permittivity (ε_r) of the different stacks through the well-known relation

$$C = \frac{\varepsilon_r \varepsilon_0}{t_{GeSe}} \quad \rightarrow \quad \varepsilon_r = \frac{C \cdot t_{GeSe}}{\varepsilon_0}$$

where *C* is the capacitance per unit area, ε_r nd ε_0 are respectively the relative and the vacuum dielectric permittivity, and t_{GeSe} is the thickness of the GeSe film. Calculations have been done considering the average value of the capacitance measured across multiple devices at 200kHz. Results are summarized in Table IV.

Sample	C @ 0V (F/m²)	$arepsilon_r$ (nominal t_{GeSe})	$arepsilon_r$ (extracted t_{GeSe})
D16 (10nm Ge ₆₀ Se ₄₀)	10.52	11.9	14.26
D21 (20nm Ge ₅₀ Se ₅₀)	4.89	11	11.73
D22 (20nm Ge ₆₀ Se ₄₀)	6.47	14.6	15

Table IV – GeSe relative permittivity as estimated from the experimental

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The value of ε_r estimated for the thinner Ge₆₀Se₄₀ sample (D16) is significantly smaller than the one obtained for the 20nm-thick Ge₆₀Se₄₀ sample (D22) when the nominal film thicknesses are considered. However, as discussed later, to reproduce accurately both I-V and G-V electrical data as a function of temperature requires to consider slightly thicker films, leading to much more consistent values of εr between the two samples (that also agree with the 14-16 range reported in literature [2], [3]). On the other hand, the relative dielectric permittivity of the Ge₅₀Se₅₀ film is found to be smaller (~12).

We then applied the DDT to the I-V and G-V data measured on D16 and D22 devices as a function of the temperature. Results are shown in Figure 12(a)-(b) and Figure 12(c)-(d), respectively.



Figure 12 – (a), (c) Current and (b), (d) conductance densities simulated (lines) and measured (symbols) at different temperatures on 10nm- (top row) and 20nm-thick (bottom row) $TiN/Ge_{60}Se_{40}/TiN$ capacitors. Since the conductance is found to be independent of the frequency, only the data measured at 2kHz are considered for the DDT.

An excellent agreement between experiments and simulations was obtained for both stacks in the whole range of voltage and temperature. The extracted material and trap parameters are reported in Table II and are extremely consistent with the two $Ge_{60}Se_{40}$ samples (as expected, since they differ only for the thickness of the chalcogenide film). Simulation results

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clearly indicate a p-type conduction through a defect band located close to $Ge_{60}Se_{40}$ valence band, as seen from the DDT defect maps reported in Figure 13. These findings well agree with the (few) reports in literature [4], [5].



Figure 13 – Defect band extracted by applying DDT on the data in Fig. 12 for (a),(b) D16 and (c),(d) D22 samples. Colored dots represent $Ge_{60}Se_{40}$ point defects (the color indicates the current driven by each trap).

The defect bands extracted from the DDT fitting D16 and D22 I-V and G-V data are located on average at ~0.82eV from $Ge_{60}Se_{40}$ conduction band bottom, i.e. at ~0.28eV from $Ge_{60}Se_{40}$ valence band top. This value is very close to the one of 0.23eV calculated in [5] for Selenium vacancies (V_{Se}), see Fig. 14.



Figure 14 – Schematic representation of the energy levels in the $Ge_{60}Se_{40}$ band-gap as calculated in [Jahangirli2011] for Germanium and Selenium vacancies and as extracted by using DDT.

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The other important trap parameter extracted with DDT is the relaxation energy E_{REL} , which is directly connected to the atomic nature of the trap and is typically derived from the temperature dependence of the charge transport (i.e. of the leakage current) [6], [7]. However, an accurate extraction of this key parameter is only possible if the observed current temperature dependence originates from the trap-assisted transport. In the case of the thick, small the band-gap GeSe layers considered here, this is not fully the case. In fact, simulations show that the charge transport occurs by means of carrier's excitation at the metal electrode/GeSe interface, and then through the defect band by means of trap-to-trap transitions. Since both processes (excitation and trap-to-trap) are strongly dependent on the temperature, the E_{REL} value of 0.3-0.5eV that is consistently extracted for the different GeSe samples has to be verified with other methods as well (for example, DFT calculations).



Figure 15 – (a) Current and (b) conductance densities simulated (lines) and measured (symbols) at different temperatures on 20nm-thick $TiN/Ge_{50}Se_{50}/TiN$ capacitors. Since the conductance is found to be independent on the frequency, only the data measured at 2kHz are considered for the DDT. (c) Defect band extracted by applying DDT. Colored dots represent $Ge_{50}Se_{50}$ point defects (the color indicates the current driven by each trap).

Figure 15 shows the comparison between I-V and G-V measured and simulated data (with DDT) as a function of the temperature on the $Ge_{50}Se_{50}$ sample D21. An excellent agreement is obtained between experiments and simulations and the extracted material and trap

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parameters are reported in Table II. The band-gap of Ge₅₀Se₅₀ is found to be larger than the Ge₆₀Se₄₀ one, which well agrees with the results obtained from DFT calculations discussed in Section 4. The defect band extracted from the DDT fitting of I-V and G-V data is located on average at ~1eV from the conduction band bottom (~0.45eV from Ge₅₀Se₅₀ valence band top), and that is also consistent with preliminary DFT calculations performed by IMEC unit (see Section 4.1). This indicates a p-type conduction, consistently with the results obtained the Ge-rich samples.

We finally applied the DDT procedure to the D23 stack, in which a 5-nm thick Carbon layer is inserted between the $Ge_{60}Se_{40}$ and the top metal electrode to act as a diffusion barrier of Ti metal that is known to degrade OTS operation after cycling.



Figure 16 – (a) Current and (b) conductance densities simulated (lines) and measured (symbols) at different temperatures on 20nm-thick $TiN/Ge_{60}Se_{40}/C/TiN$ capacitor. Since the conductance is found to be independent on the frequency, only the data measured at 2kHz are considered for the DDT. (c) Defect band extracted by applying DDT. Colored dots represent $Ge_{60}Se_{40}$ point defects (color indicates the current driven by each trap).

Experimental I-V and G-V are nicely reproduced by considering the same $Ge_{60}Se_{40}$ material and trap parameters extracted by means of DDT from D16 and D22 samples, thus proving the reliability of Defect Discovery Tools.

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	D16 (10nm Ge ₆₀ Se ₄₀)	D22 (20nm Ge ₆₀ Se ₄₀)	D21 (20nm Ge ₅₀ Se ₅₀)	D23 (20nm Ge ₆₀ Se ₄₀ /5nm C)			
Parameter	Ge ₆₀ Se ₄₀	Ge ₆₀ Se ₄₀	Ge ₅₀ Se ₅₀	$Ge_{60}Se_{40}$	Carbon		
t _{GeSe} (nm)	12	20.5	21.3	20	7		
E _G (eV)	1.1	1.1	1.45	1.1	2		
WF _{TE} (eV)	4.65	4.65	4.65	4.7			
WF _{BE} (eV)	4.65	4.65	4.65	4.65			
m [*] _{tunn,e/h} /m ₀	0.43	0.47	0.44	0.43	0.6		
Е _т (eV)	0.835	0.81	1	0.835	-		
ΔE_{T} (eV)	0.226	0.23	0.18	0.226	-		
E _{REL} (eV)	0.306	0.47	0.42	0.3	-		
N _⊤ (cm ⁻³)	3.17·10 ¹⁹	5.5·10 ¹⁹	6.2·10 ¹⁹	$3.17 \cdot 10^{19}$	-		

Table V – Material and trap parameters extracted using the DDT to reproduce I-V and G-V data measured as a function of temperature on the different OTS devices.

3. DFT Calculations

This section describes the DFT calculations performed by the different project units CNR, ICN2 and IMEC, with the aim of providing an atomistic understanding of the structureelectronic interplay of OTS amorphous chalcogenides. Particular attention is given to (i) electronic structure characterization, and to the identification of the defect-like structures responsible for the electrical traps in the mobility gap of the GeSe-based materials, (ii) the characterization of the metal/amorphous TiN/GeSe interfaces that constitute the basic elements of the MIM device described above.

3.1 Preliminary Characterization of GeSe Electronic Properties

The prerequisite to study the electrical properties of amorphous materials is the identification of reliable atomic structures. However, there is insufficient information available about the structural properties of these GeSe amorphous materials to date, either from experiments or from theory. In absence of specific experimental results about the glassy phase at room temperature, we aim at developing realistic amorphous models by carrying out an extensive set of independent simulations obtained with different multi-scale techniques and different codes. The activity proposed here is focused on the first principles side, in order to obtain atomistic models of the amorphous structure, without resorting to experimental information or adjusted interatomic potentials. These models will be the starting point for future studies concerning the behavior of the materials in presence of external fields (the electrical cycling of the device) defects and dopants, which determine the device properties and the material suitability for memory selectors.

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We first made a complete validation study on the crystal phase of stoichiometric GeSe. A particular effort was devoted to characterize the accuracy level obtained with different localized basis sets, as these are used by the SIESTA [8, 9] and the CP2K [10] codes used in many of the subsequent studies of the amorphous phases. Both codes use a basis set of atomic orbitals, which are the product of a radial function and a spherical harmonic to describe the angular dependence. The choice of how many orbitals per atom are used to describe the electronic wavefunctions is an important one, as the balance between accuracy and computational cost critically depends on it: while a large number of orbitals provides very accurate results, they also require heavier computational costs. Our preliminary tests focused on determining what size of basis set is sufficient to provide an acceptable accuracy, while minimizing the computational demands.

The calculations of the basis set convergence have been made with the SIESTA code, but the conclusions also apply to those performed with CP2K. The main result is summarized in Table VI. *SZ*, *DZ* and *TZ* indicate single- double- and triple-Z basis sets (containing one, two and three different radial functions for each angular momentum components occupied in the free atom, respectively). *P*, *DP* and *TP* stand for polarized, double-polarized and triple-polarized, which indicate the addition orbitals with one more angular momentum component than the ones occupied in the three atoms (with one, two and three radial functions, respectively). *+f* indicates the addition of a shell of *f* orbitals to polarize the d states. The results of Table VI indicate that the *DZP* basis is an optimal one, providing a total energy close to the one obtained with the most complete basis set (*TZTP*), while containing only 13 orbitals per atom (2 shells of *s* states, 2 shells of *p* states and one shell of *d* states). This basis will be used in the remaining work, whenever local orbitals are used as a basis set. Basis set convergence is less critical in Quantum Espresso (QE)QE, where accuracy convergence is reached by increasing the number of planewaves which constitute the basis set.

Table VI – Basis set convergence: Total energy for the unit cell of the GeSe crystal, as a function of the size of the basis set. Calculations are done with SIESTA, using the DRSLL van-der-Waals Density Functional [38]. Similar results are obtained with either LDA and GGA functionals.

Basis Set	Total Energy (eV)
SZ	-1.821.169,435
SZP	-1.823.161,862
DZ	-1.822.303,889
DZP	-1.824.094,737
DZDP	-1.824.316,404
DZDP+f	-1.824.449,331
TZ	-1.822.578,579
TZP	-1.824.240,501
TZDP	-1.824.475,278
TZTP	-1.824.544,012

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As a first step for the description of the amorphous materials, we carried out preliminary DFT simulations, by using the CP2K [10], which allows for a fast and reliable characterization of the ground-state properties of the GeSe amorphous system. These calculations employ Goedecker, Teter and Hutter pseudo-potentials [11, 12], and localized basis sets (of DZT quality) in the PBE (Perdew-Burke-Ernzerhof) implementation of Generalized Gradient Approximation to exchange-correlation (XC) functional [13]). Several sizes were tested for different purposes, ranging from 1nm to 5nm models: smaller (1nm) models are used to illustrate the minimum requirements on the model size for quantitative electronic structure simulations, larger (5nm) models are used in electric field simulations, whereas the 2-3nm models are optimal to investigate the electronic properties. Melt-and-quench simulation protocol is used to generate the amorphous models. This includes 3-temperature steps: first, initial models are melted at 1200K, then they are guenched at 800K and 400K with a fast pressure-release step between quenching steps. With such an algorithm, the 2x2x2nm models were generated in 27-36ps simulations. Finally, a full system relaxation is performed. A hybrid method (HSE functional [14]), in combination with the Auxiliary Density Matrix Method (ADMM), is used to quantify the electronic structure on 10 samples of 2x2x2nm size [15]; results are similar on a 3x3x3nm sized model. Inverse Participation Ratio (IPR) for each state in the amorphous model is calculated to define the edges for the mobility gap.

In order to have a statistical representation of the electronic properties of the amorphous system, we considered 10 different atomic models, and calculated the corresponding density of states (DOS). Results are summarized in Figure 17, where single DOS spectra are aligned at the valence edge of the mobility gap.

In the Se-rich models (a-Ge₃₀Se₇₀), we find many deep electron traps, reaching 2/3 of the gap, which is the largest gap amongst the three given concentrations. The a-Ge₅₀Se₅₀ elemental alloy displays a median mobility gap of 1.05 eV, with shallow hole traps and deep electron traps that reach the mid-gap. With Ge-content 70%, the mobility gap of the GeSe chalcogenide is the gap of pure Ge (0.7 eV): Ge-related states define both conduction and valence mobility edges. Models contained many gap states, on average the hole traps located in the middle of the gap, electronic traps reach only down to a third of the gap.

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Figure 17 – Electronic structure of the amorphous Ge_xSe_y , x=30,50,70%, y= 70,50,30%. Median mobility gap (colored big boxes Eµ) with overlapped statistical boxes for the deepest electron traps (blue arrow pointing down from the Conduction Edge) and hole traps (red arrows pointing up from the Valence Edge)

A more detailed analysis was performed on the 10 different atomic models obtained for stoichiometric a-GeSe, using the SIESTA code. The electronic Density of States (DOS) is shown in Figure 18. One of the most interesting features of these results is that all the samples show a pronounced suppression of states around the Fermi level, resembling the semiconducting character of the parent crystalline phase. A close look around the Fermi level (Figure 18, right panel) shows that some of the samples display a clean gap, while others contain a small number of states within the band gap. Further analysis shows that these are all states which are localized around coordination defects in the amorphous structure. In particular, they are typically associated to atoms which are under- or over-coordinated with respect to the ideal crystalline local structure, where all the atoms are three-fold coordinated: each Ge atom is bonded to three Se atoms, and each Se is bonded to three Ge atoms. In the amorphous phase, we find atoms with have a larger or smaller number of neighbors, and also some Ge-Ge pairs which are not present in the crystal phase. In our calculations, we have observed that the Ge-Ge pairs do not seem to induce the presence of states in the bandgap, whereas over/under-coordinated atoms do. An example is shown in Figure 19, where the charge distribution of the states within the bandgap is shown in real space. We see that the states are strongly localized around a small number of atoms. Further analysis shows that these atoms correspond to a Ge atom, which is overbonded to 5 Se atoms, and to a Se atom which is underbonded to 2 Ge atoms.

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Figure 18 – Electronic Density of States (DOS) for the 10 models of a-GeSe, obtained with SIESTA and the DRSLL van-der-Waals Density Functional. The left panel shows a broad energy window, showing most of the valence states and some of the unoccupied states. The right panel shows a zoom around the Fermi level (located at 0.0 eV).



Figure 19 – Left: Density of States around the Fermi level (at 0.0 eV) for one of the structural models of a-GeSe. Right: Charge density associated to the states within the band-bap for the same structural model, showing that the states are strongly localized.

Starting from these preliminary results, we carried out an extensive set of simulations to identify how the structural and electronic properties of the amorphous models depend on numerical parameters such as codes and computational details (e.g. basis set, XC-functionals, pseudopotentials, etc.), initial structures, model size, and quenching-melting algorithm. We used both QE [16] and SIESTA [8, 9], that are the two DFT codes included in the IM2D platform developed within the INTERSECT project. The use of both QE and SIESTA allows us to enlarge the portfolio of physical properties, compositions and system sizes that can be addressed, and to obtain independent results which can be compared for a more robust, unbiased and feasible model of amorphous GeSe system.

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As an initial benchmark test, we started from the same 10 model structures for the Ge_{0.50}Se_{0.50} alloy described above (hereafter indicated as INI) and we re-calculated the electronic structure of the system (no atomic relaxation), by using both the QE and the SIESTA codes. Both of them produce virtually identical results, and therefore only those obtained with QE are discussed here for simplicity. QE provides a plane-wave, pseudopotential implementation of the DFT problem. Hybrid HSE XC functional is used for scf electronic structure calculations. Results are summarized in Figure 20a (red lines) and perfectly reproduce the results obtained with the CP2K code at the same level of accuracy (i.e. XC=HSE). In order to check the effect of the XC choice, we re-calculated the electronic structure of the same amorphous systems by using a DFT+U approach, namely ACBNO [17], that has been proved to correct the band gap underestimation of standard DFT calculations with a reduced (with respect to hybrid functionals) computational cost. The effective U values for both Ge (U=0.16 eV) and Se (U=2.28 eV) species have been calculated in the GeSe crystalline phase. The results are also included in Figure 20a (green lines) for comparison. DFT+U well reproduces all the spectral features of the HSE simulations, while the band gaps are systematically smaller than HSE ones by ~0.1 eV. This confirms that DFT+U approach represents an accurate low-cost solution, alternative to hybrid functional, for large-scale electronic structure simulations.



Figure 20 – Density of states of representative models of amorphous Ge_{0.50}Se_{0.50}. Left: Comparison between HSE (red) and DFT+U (green) simulations on initial (INI) structures. Right: Comparison between initial (red) and MD-evolved (purple) structures simulated using hybrid HSE XC functionals. Zero energy reference is set to Fermi energy of each system.

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The second aspect that we analyzed is the effect of the melting-quenching and relaxation protocol adopted above to obtain the amorphous models. We started from the same 10 configurations, and we let each system evolve for 10 ns by using classical Molecular Dynamics (MD) simulation tool in the microcanonical simulation ensemble (i.e. temperature is not controlled). This is expected to maintain the main glassy structure of the systems (as resulting from the melting-quenching) but removing the details of the final relaxation step. Finally, a self-consistent DFT (XC=HSE) run is performed to calculate the DOS. Figure 20b shows the comparison between the DOS plots of the initial (red) and MD-evolved (green) structures. The results indicate that, even though each model has an open band gap at the Fermi energy, the details (e.g. number and energy position) of defects states have changed *wrt* to the initial configurations. This confirms the delicate role of the simulation procedure in the definition of the structural and electronic properties of amorphous systems.

Finally, we considered the effect of the quenching-melting step, used to generate the amorphous model. Starting from configuration **0** of Figure 20, we performed an ab initio molecular dynamics simulation, by using the Car-Parrinello (CP) molecular dynamics, as implemented in the QE package. The exchange-correlation functional is described by using the vdW-DF2-B86R formulation [18] of generalized gradient approximation, which includes Van der Waals corrections to describe non-bonding interactions. We performed a melting-and-quenching amorphization cycle, by melting the system at 1500K for 15 ps, followed by a cooling down step to 300K, with a rate of 100K/ps. After quenching, a production run conducted at 300K for 15 ps.

The resulting radial distribution function g(r) plots, shown in Figure 21a, well reproduce the characteristic first-neighbor bonding distribution within the Ge_{0.5}Se_{0.5} system. Other ten atomic structures are extracted by the CP trajectory at room temperature, and used as models to sample the DFT electronic structure (DFT+U) of the amorphous system. Figure 21b shows the average DOS (black) and the IPR (green) functions. The results are in good agreement with the initial preliminary calculations: The average model has a mobility gap of ~1.0 eV partially filled by localized states, as demonstrated by the analysis of the single particle electronic structure in panel c.





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Figure 21 – Radial distribution function, g(r), for the amorphous phase at 300K for each Ge_{0.5}Se_{0.5} system, from ab initio CP simulations. (b) Average DOS (black line) and IPR (green dots), obtained sampling 10 configurations, extracted from the CP trajectory at room temperature. Dashed orange lines identify the edges of the mobility gap. (c) Single particle electronic structure analysis of a selected configuration.

In order to gain insights on the origin and the details of defect states, discussed in transport models of Sec. 3.3, we studied the short-range (e.g. folded structures) and the medium-range (e.g. rings and network connectivity) local-order structures within the simulation cells. In analogy with other chalcogenide systems, it is expected that the presence of gap/tail states is related to under/over-coordinated Ge atoms [19, 20], and to the ratio of homopolar/heteropolar bonds in the sample [21]. In particular, the formation of lowcoordinated Ge-structures and Ge-Ge chains would acts as effective Se-vacancy defects in the electronic structure of the system (in agreement with the analysis of Sec. 3). The visual analysis of localized in-gap states (Figure 21c) seems to confirm this interpretation. However, in order to have a quantitative characterization of these features, we implemented an original code, named BELLO (Bond Element Lattice Locality Order), designed for the automatic analysis and the extraction of main structural characteristics of disordered systems. This includes the calculation of local-order parameter q, statistics and PDB/XYZ formats, detailed atomic coordination number and pair/angle-distribution functions. The main features of this code are reported in a joint (CNR and AMAT) manuscript to be submitted for publication [22].

The main short-range folding structures for CP models were compared with a large scale (>4600 atoms) classical MD simulations. The use of classical MD raises up the possibility to study extended systems with thousands of atoms for several nanoseconds, which allows for medium-range spatial order organization. Particularly relevant is the time required for reliable melting-quenching annealing cycles (>20ns) necessary to generate the amorphous glasses, which is usually not accessible to first-principles simulations. The comparison between CP and MD structural analysis is shown in Table VII and Figure 22. Ab initio CP models have a predominant distribution of low-folded structures (0-3 folded) that are characteristic of the melt phase, while higher folded aggregation are minor components, in evident contrast with the classical MD results at the same temperature. Computational

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limitations on system size and simulation time (especially quenching step) do not allow the ab initio model to proper cool down and aggregate in highly-folded structures, typical of the glass phase. This may affect the number and the spatial distribution of mis-coordinated Ge atoms, and thus the presence of trap states in the amorphous band gap. These results are collected in a paper submitted for publication [23].

Table VII – Average percentage of folded structures in $Ge_{0.50}Se_{0.50}$ alloy, from ab initio CP and classical MD simulations at 300K.

	0-FOLD	1-FOLD	2-FOLD	3-FOLD	4-FOLD	TETRA- HEDRAL	5-FOLD	OCTA- HEDRAL
СР (300К)	0,77%	21,93%	39,10%	33,85%	2,84%	1,22%	0,29%	0,00%
MD (300K)	0.9%	6.7%	16.0%	23.6%	25.6%	0.3%	18.5%	8.4%



Figure 22 – Pie chart distribution of folded structures from ab initio CP and classical MD simulations at 300K [23].

The massive set of tests and calculations presented in this Section - carried out by using different approaches, codes and model systems - allowed us to identify the most relevant computational and physical aspects that affects the structural and electronic properties of amorphous chalcogenides. Main results are: (i) electronic structure deeply depends on the protocol used to generate the amorphous (e.g. melting-quenching, relaxation); (ii) All the considered amorphous structures have a mobility gap of 1.0 eV (DFT+U) - 1.2 eV (HSE), in agreement with the experimental data (see above); (iii) Occupation of the mobility gap by localized states depends on the details of the atomic structure (e.g. local order distribution). On the basis of these results we started a large set of DFT calculations for the characterization of Ge_xSe_{1-x} amorphous systems at different stoichiometries ($0.4 \le x \le 0.6$) and in the presence of dopants, for a direct comparison with the experimental counterpart and the generation of materials data for GinestraTM simulations. To this aim, ICN2 and CNR submitted a joint computational project (P.I. P. Ordejón, ICN2) to Spanish HPC center RES.

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The project (ID FI-2020-2-0037) has been awarded and the resources have been allocated. Simulations will be performed in the next months.

3.2 TiN/GeSe interface

The selector devices described in Sec. 3 are based on two-terminal MIM structures, such as TiN/GeSe/TiN, whose electrical response is dominated by the TiN/GeSe interfaces. While the intrinsic properties of the OTS chalcogenide materials are partially characterized by experimental and theoretical studies (see e.g. Sec 4.1), an atomistic investigation of the metal/semiconductor interface is missing.

One key feature in the realization of MIM devices is the alignment between the work function (WF) of the metal contact and the semiconductor band edges. It is generally assumed that TiN has a WF = 4.7 eV, even though this value can be modulated over a large energy range 4.1-5.3 eV [24, 25], depending on growth characteristic of the sample, the coupling with semiconductor (e.g. doped Si) or metal-oxides substrates (e.g. HfO₂, Al₂O₃) or temperature treatments. Here, we considered two main aspects: (i) the intrinsic structural origins of the WF variability, and (ii) the explicit description of the a-GeSe/TiN interface.

3.2.1 TiN work function

TiN crystallizes in a cubic rocksalt structure, and can be easily cleaved along several low-index faces, such as (110), (110), and (111) surfaces. Previous works indicated a net trend in the surface formation energy of the cleavage surfaces, where (100) is the most and (111) is the least stable one [26]. Nonetheless, the growth of single crystal films is unusual and too expensive for any realistic technological application. Almost all TiN-based electrodes, including those reported in section 3, are made of polycrystalline films, whose constituting grains have different sizes and expose multiple faces depending on the conditions and techniques used to grow the samples. In standard growth conditions (i.e. N-poor) TiN forms stable non-stoichiometric crystals (namely TiN_x) over a broad composition range x [0.3, 1.2] [27]. A large variety of multi-technique experiments [28, 29] indicate that in substoichiometric TiN_x the most recurrent defects are the nitrogen vacancies V_N, and that high V_N concentrations remarkably affect the optoelectronic [30] and the transport properties of the system, including its WF [31].

In order to unravel the origin of the large WF variability observed experiments, we carried out a first principles study of the effect of surface termination and stoichiometry of the WF TiN surfaces. TiN surfaces are simulated by periodic supercells, where we included a thick vacuum layer (15Å) in the directions perpendicular to the surface. Each slab contains a variable number of layers with (100), (110) or (111) surface orientation, which cover the thickness range 1.0-4.0 nm (Figure 23a). (100) and (110) faces expose an equal number of Ti and N atoms, while (111) surfaces are terminated either with Ti or with N atoms at both slab

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ends. In standard N-poor growth conditions, Ti-terminated surface has the lowest surface energy [32]. The work function for all systems is calculated as the difference between the Fermi energy resulting from DFT calculation, and the vacuum level, extracted from the double averaged electrostatic potential [33]. Results (Figure 23b) clearly indicate the effect of the surface termination on the WF of TiN. The calculated WF values are 2.96 eV, 3.17 eV and 4.67 eV for TiN(100), TiN(110) and TiN(111), respectively. Thickness hardly affects the WF, that for all surface orientations remains almost identical with respect to the number of layers (Δ WF=30 meV). These results are well representative of polycrystalline films used in experiments (Sec. 3), where the typical grain size is of the order of few nanometers.



Figure 23 – (a) Side view atomic structure of TiN surfaces, with (001), (110) and (111) orientation and thickness ranging from 1 nm to 4 nm. (b) Calculated work function for TiN(100), TiN(110) and TiN(111) surfaces, at variable thickness. (c) WF function of TiN_x in the presence of multiple N vacancies (V_N). The corresponding values for undefective TiN surfaces (dashed lines) are reported for comparison [34].

The calculated WF s of defective TiN_x surfaces are shown in Figure 23c. When the Ti/N ratio increases, WF deviates from the stoichiometric value. Work function of $TiN_x(100)$ increases while WF of $TiN_x(111)$ decreases by hundreds of meV. As the amount of N content is reduced, the WF of both TiNx surfaces approaches the value WF =4.2 eV, which is the fingerprint of the Ti hpc-metal. This analysis indicates that single WF values, deriving from experiments and used in transport models, are instead averaged sample results instead, where the surface terminations and the chemical composition play a combined role. The statistical predominance of (111) surface [24, 25] pins the final value close to WF=4.6 eV. TiN(100) has lower WF but the presence of N-vacancies shifts WF to higher energy values closer to the (111) surface. We can conclude that the overall WF value of polycrystalline electrode depends on the specific percentage of exposed grain faces and of their composition, and thus on the specific growth conditions. These results have been collected in a paper recently submitted for publication [34].

3.2.2 TiN/GeSe interface

We considered four interfaces constituted of 1nm-thick layer of TiN(100) with (4x4) lateral periodicity and 1nm-thick layer of amorphous $Ge_{0.50}Se_{0.50}$, as shown in Figure 24a. The four

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interfaces differ in the atomic structure of the chalcogenide layer, extracted from different DFT configurations, among those studied in Sec. 3.1. This allowed us to understand the role of the amorphous structures on the electronic properties of the metal/semiconductor interfaces. All systems have been fully relaxed until the forces on each atom was lesser than 0.03 eV/Å. The electronic structures have been calculated at the DFT+U level, by using the same U parameters discussed above. Effective Screening Medium Method [35] has been applied to cancel the spurious electric dipole that would be generated across the vacuum region of the repeated simulation cells, due to the inequivalent nature of the exposed slab sides (i.e. TiN and GeSe). The resulting electronic structures are shown in Figure 24b. The detailed band alignment plot for configuration **1** is shown in Figure 25.



Figure 24 – Side view atomic structure (a) and projected DOS (b) of four a-GeSe/TiN(100) interfaces. Vertical dashed line identifies the Fermi energy (E_F).



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Figure 25 – Band alignment of a-GeSe/TiN(100) (model 1). All energies are referred to vacuum level, assumed as the zero energy reference. Black thick line identifies the Fermi level of the final interface. Fermi level of isolated TiN (blue) and the band edges of the isolated GeSe layer (orange) are superimposed for comparison. WF and Ip are the work function of TiN and the ionization potential of a-GeSe, respectively. Dashed orange lines represent the localized defect states within the mobility agp^mE_n.

All systems form a Schottky barrier at the interface, with the Fermi level of TiN metal laying in the mobility gap of the amorphous GeSe layer. The specific distribution of localized states in the mobility gap (Sec. 3.1) are responsible for the minor differences in the DOS plots of Figure 24b. In the specific case shown in Figure 25 (model 1), the final Fermi level is set close to the valence band edge and in proximity of several occupied and empty trap states available for transport. The formation of the interface causes an average blue shift of the TiN(100) work function to 4.9 eV.

Finally, since TiN easily undergoes surface oxidation [36], we considered the effect of an oxide interlayers in the TiN/GeSe interfaces. Following the experimental indications [37], we prepared the initial O:TiN(100) structure by including a combination of N-substitutional O atoms and O_2 adsorbed molecules to the TiN(100) surface. This structure has been demonstrated [37] to correctly reproduce the optoelectronic experimental properties of O:TiN films. A 1nm-thick layer (as in model 1) is finally added on top of the O:TiN(100) surface, and the interface has been fully relaxed. Final atomic and electronic structures are displayed in Figure 26.



Figure 26 – (a) Side view atomic structure, (b) projected , and (c) band alignment plots of a-GeSe/O:TiN(100) Labels follow Figures 22 and 23.

On one side, oxygen interacts with TiN surfaces, saturating exposed N-vacancies and bonding to outermost Ti atoms. This leads to the formation of TiN_xO_y layers with different Ti

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coordinations: one intermediate mixed Ti-O-N layer and one Ti-O external capping layer, in agreement X-ray experimental analysis [36], [acs_37]. On the other side, oxygen strongly bonds to Ge atoms, forming a Ge-O submonolayer. Even though O-derived states results to be far away the Fermi energy (panel b), the oxide layer remarkably modifies the TiN/GeSe interface and the corresponding band alignment (panel). Metal oxidation imparts a drastic shift by 4.1 eV of the TiN(100) work function (red line). The formation of the interface with the a-GeSe layer partially cancels this effect, setting the work function of the entire system (black line) at =5.1 eV. We can conclude that, the possible oxidation of the electrodes, which can take place e.g. upon air exposure, can cause a small but not negligible shift of a few hundreds of meV in the TiN/GeSe work function. These analyses will help refinement of the transport models, used in the device MIM simulations (Sec. 3).

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ACRONYMS

- ADMM Auxiliary Density Matrix Method
- BELLO Bond Element Lattice Locality Order
- **BEOL** Back End Of Line
- CP Car Parrinello
- DDT Defect Discovery Tool
- **DFT** Density Functional Theory
- DOS Density of States
- HPC High Performance Computing
- IM2D Interoperable Materials-to-Device
- **IPR** Inverse Participation Ratio
- MD Molecular Dynamics
- MIM Metal Insulator Metal
- **OTS** Ovonic Threshold Switching
- PVD Physical Vapor Deposition
- QE Quantum Espresso
- WF Work Function
- XC Exchange-correlation functional

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