D3.1

Atomic defect properties from the electrical measurements on FE-HfO_2-devices

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Disclaimer:

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D3.1 Atomic defect properties from the electrical measurements on FE-HfO_2-devices

Contents

[1] Acronyms are marked in purple in the text and defined at the end of the document.

Executive Summary

This document provides a description of the use of the *device cycle* of the IM2D Simulation box to extract material and defect properties from the interpretation of the electrical data measured on ferroelectric devices. It is developed within Work Package 3, "Testing and piloting", and its task n. 3.1, "FE-transistor and FE-memories: Extraction of defect properties from electrical measurements", with IMEC as task leader and contribution from CNR, ICN2, EPFL, MDLab, FMC, IMEC.

The task activities rely on the use of the Defect Discovery Tool (DDT) functionalities implemented into AMAT proprietary Ginestra^{TM} platform, which are specifically developed to extract intrinsic material/device properties (e.g. bandgap, thicknesses, etc.) and characteristics of the defects (e.g. thermal ionization and relaxation energies, distribution within the bandgap) from electrical measurements.

DDT functionalities are applied to current-voltage and threshold voltage shifts (ΔV_T), characteristics measured respectively on Silicon-Ferroelectric-Silicon (SFS) capacitors and high-k/metal gate (HKMG) ferroelectric transistors with doped FE-HfO_2. Devices and electrical measurements are provided by IMEC and FMC units.

Consistent results are obtained for the data and devices considered and show that both charge transport and ΔV_T are originated by a different trap state with respect to the ones typically reported for conventional HfO_2. The similarities found between the properties, extracted by using the DDT for the defects in doped HfO_2 of both SFS and HKMG devices, suggest that these traps may be related to specific features of the FE-HfO_2 structure that are at the bases of the ferroelectricity in this material.

1. Introduction

One of the goals behind the INTERSECT project is to setup an Interoperable Materials to Device (IM2D) framework able to integrate materials modelling codes in a way that permits mutual interaction and exchange of information. In order to test the IM2D simulation box infrastructure, AMAT and the other project units identified two pilot cases to be used for piloting and testing (see DoA): one on chalcogenide-based selectors, and one on ferroelectric-based devices.

This "Atomic defect properties from the electrical measurements of FE-HfO2-devices" report focuses on the pilot case for the development of solutions for FE materials. Results for chalcogenide pilot are reported in Deliverable D3.2. More specifically, the present report addresses the device-to-material workflow, that is the extraction of defects properties from electrical measurements. On one hand, the main physical aspects related to this piloting problem will constitute the input for the formalization of use cases, and their translation into interoperable workflows will be done within WP1 activities and implemented within WP2 activities. On the other hand, calculations will be performed using the beta versions of the code that are implemented in WP1-2 during the project.
This document specifically describes the status of Deliverable D3.1, concerning the application of the IM2D toolbox to the pilot case of Ferroelectric (FE) HfO_2 devices.

2. Extraction of FE-HfO_2 atomic defect properties

2.1 Devices and Experimental Data

Devices and measurements used for the activities of Task 3.1 have been provided by IMEC and FMC units and constitute two independent and complementary sets of data, which allows us a deeper comprehension of such complex systems.

2.1.1 Silicon-Ferroelectric-Silicon (SFS) Samples

The devices fabricated by IMEC unit are Al-doped HfO_2 capacitors (IMEC wafer AL803394D02), also described in [1] (Fig. 1). The gate stack structure was Poly-Si/FE-HfO_2 (8 nm)/Si substrate. The Si substrate and Poly-Si gate were highly p-type and n-type doped, respectively. The FE-HfO_2 was deposited by atomic layer deposition (ALD) with Al as dopant. Post-deposition, annealing for 1 min at 850°C in N_2 ambient was performed to crystallize the FE-HfO_2. The 300 mm wafer is divided into 326 dies, each of which was patterned with IMEC "CAPA2" mask-set. The area of measured capacitors was 50 µm×50 µm.

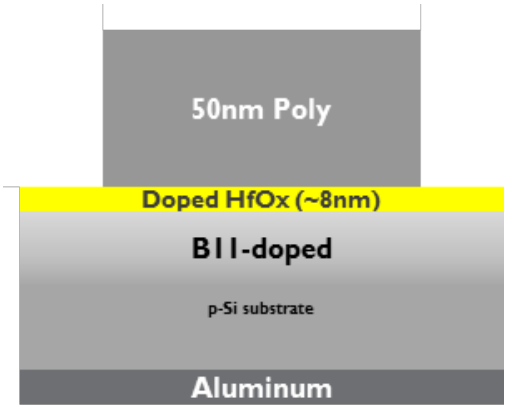


Figure 1 - Schematic cross-section of the FE sample.

The samples were measured at the following conditions:

- Before cycling
- After cycling (Up/Down State)
- Cycling + Baking (Up/Down State)

Here, "*cycling*" means 100 cycles of triangular pulses with segment amplitudes of 0 V, -4 V, +4 V, 0 V (rise time 100 µs) resulting in the ferroelectric layer being left in the "Down" state, or 0 V, +4 V, -4 V, 0 V resulting in the ferroelectric layer being left in the "Up" state. "*Baking*" means 1hr at 150°C in an oven.

I-V curves "Before cycling" were measured at the multiple temperatures, while C/G-V-f measurements were carried out at room temperature only. The following parameters were used:

I-V characteristics:

- Keithley 2602A
- V swept from 0 to -3 V or from 0 to +3 V
- Step delay of 2 s to suppress transient current
- T = 25 – 85 oC

C/G-V-f characteristics:

- Agilent E4980A LCR
- V swept from 0 to -2.4V or from 0 to +2.4 V
- f range 20 Hz – 2 MHz (log distributed)
- small signal Vac = 30 mV
- CPG model enabled
- Room temperature only

Each (I-V or C/G-V-f) measurement was performed on an individual device. 24 devices were measured at each measurement condition at RT. 12 devices were measured at each measurement condition at 55 °C and 85 °C. Results were afterwards overlaid to identify typical behavior and the outliers were manually censored out.

The I-V, C-V-f and G-V-f measurements of the capacitors Before cycling, After cycling ("Up" and "Down" states) and After Baking ("Up" and "Down" states) are shown in Figs. 2-4. From Fig. 5 it is apparent that both cycling and baking have impact on leakage characteristics, as does the state ("Up" or "Down"). Such impact is also visible in both C-V and G-V characteristics (Fig. 6).

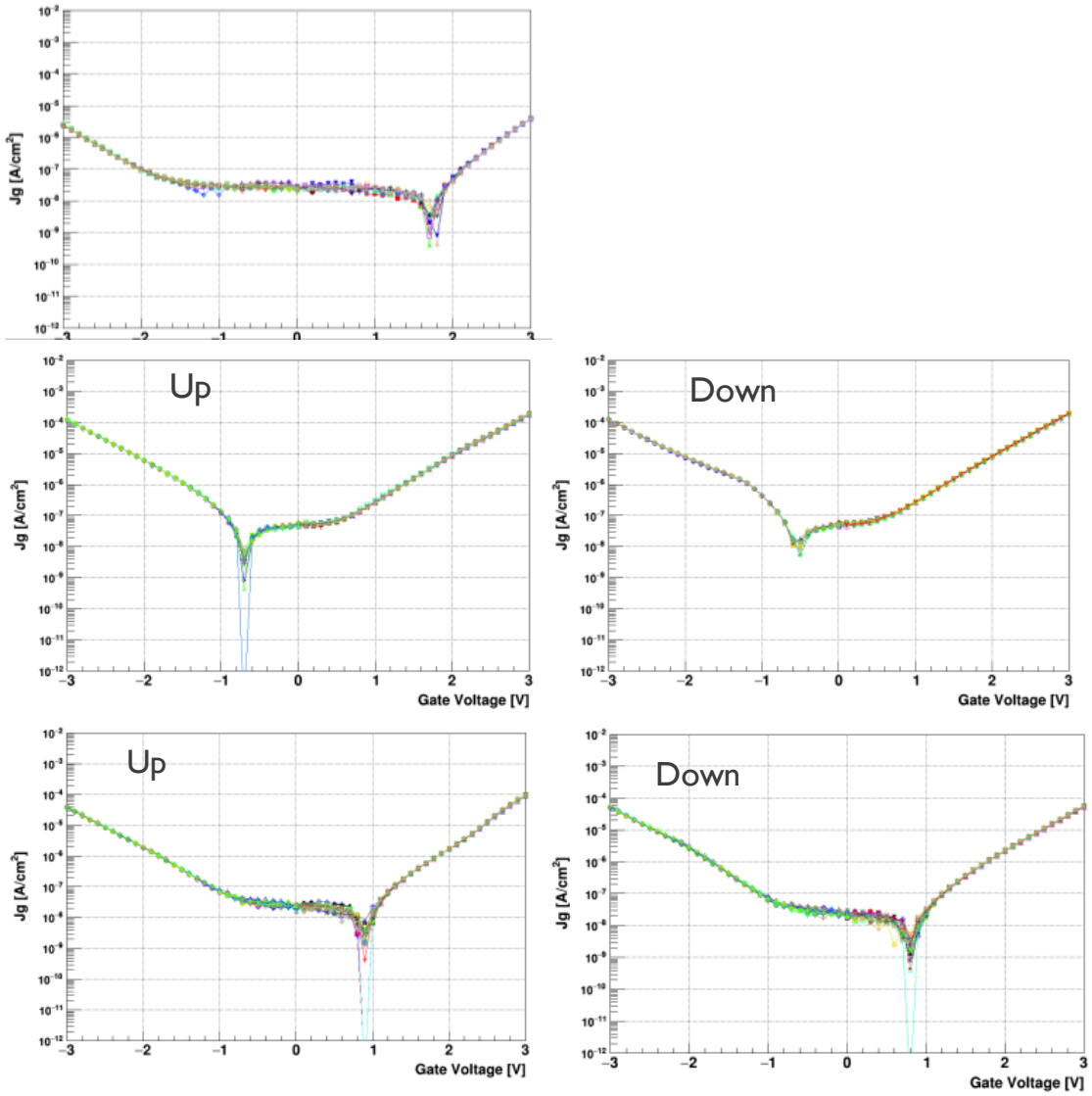


Figure 2 - I-V characteristics measured on multiple devices (top row) Before cycling (middle row) After cycling ending with Up and Down polarizations (measured after 1day at RT) (bottom row) After Baking (Up and Down polarizations).

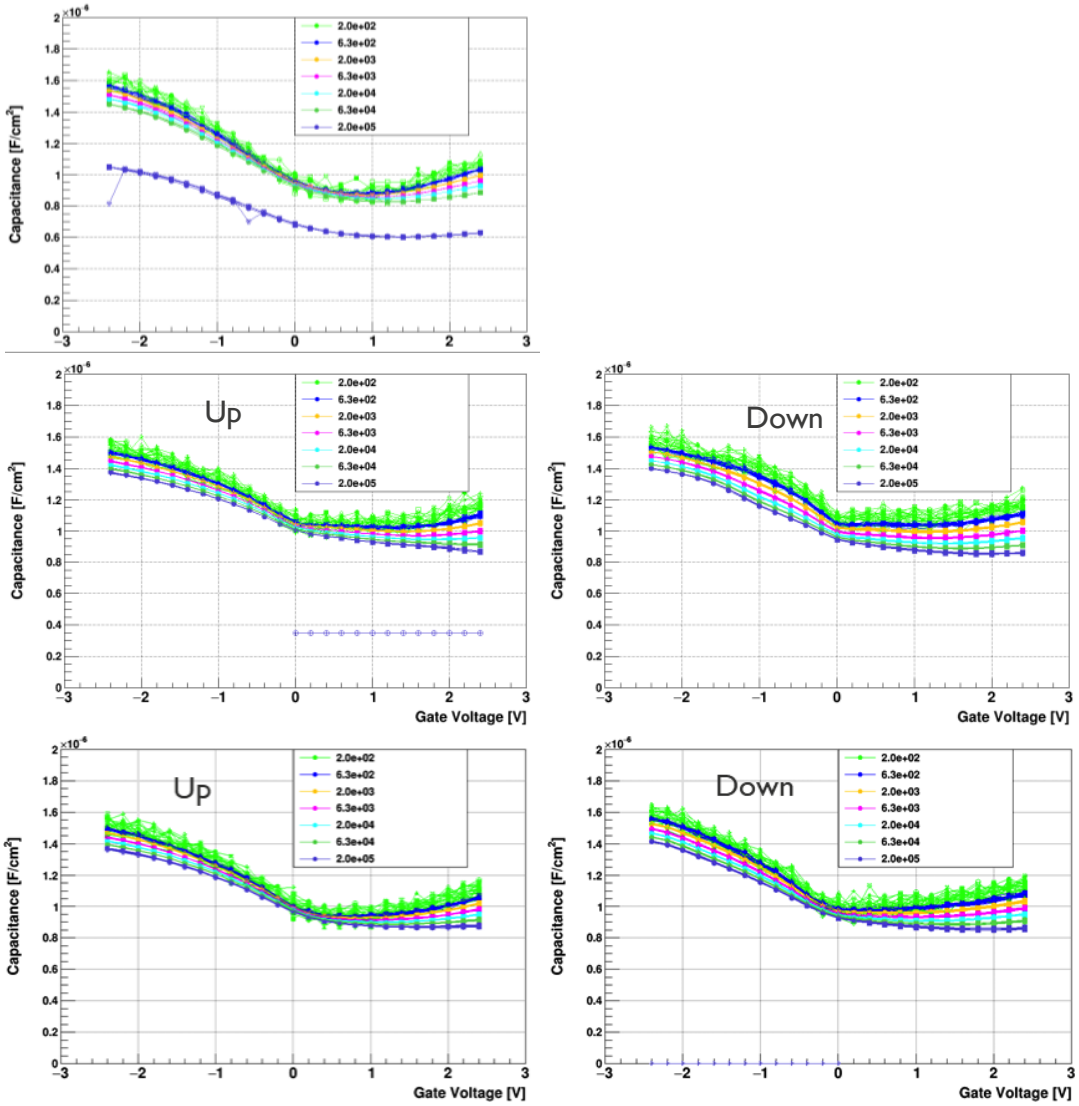


Figure 3 – C-V-f characteristics measured on multiple devices (top row) Before cycling; (middle row) After cycling ending with Up and Down polarizations; (bottom row) After Baking (Up and Down polarizations).

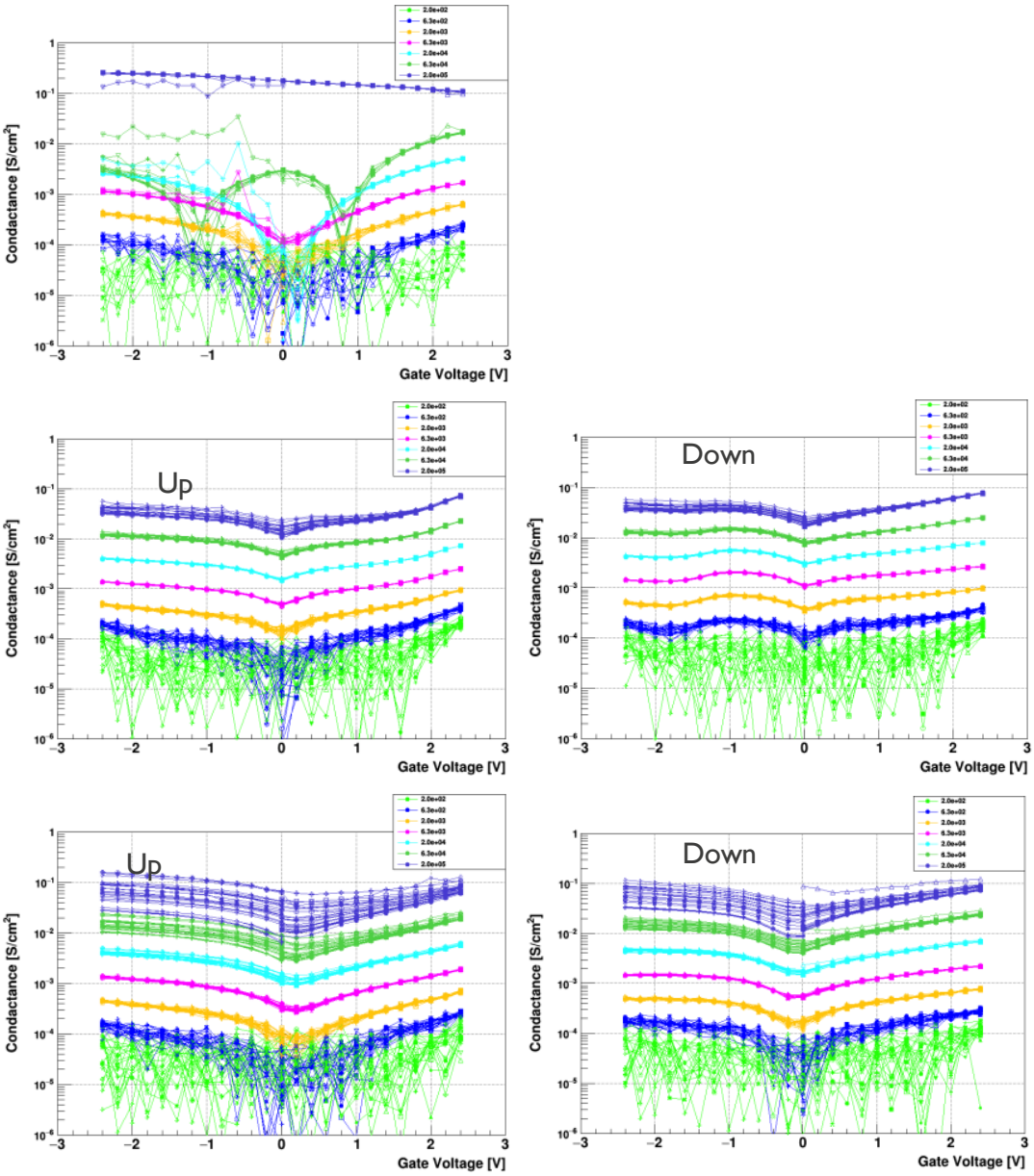


Figure 4 – G-V-f characteristics measured on multiple devices (top row) Before cycling; (middle row) After cycling ending with Up and Down polarizations; (bottom row) After Baking (Up and Down polarizations).

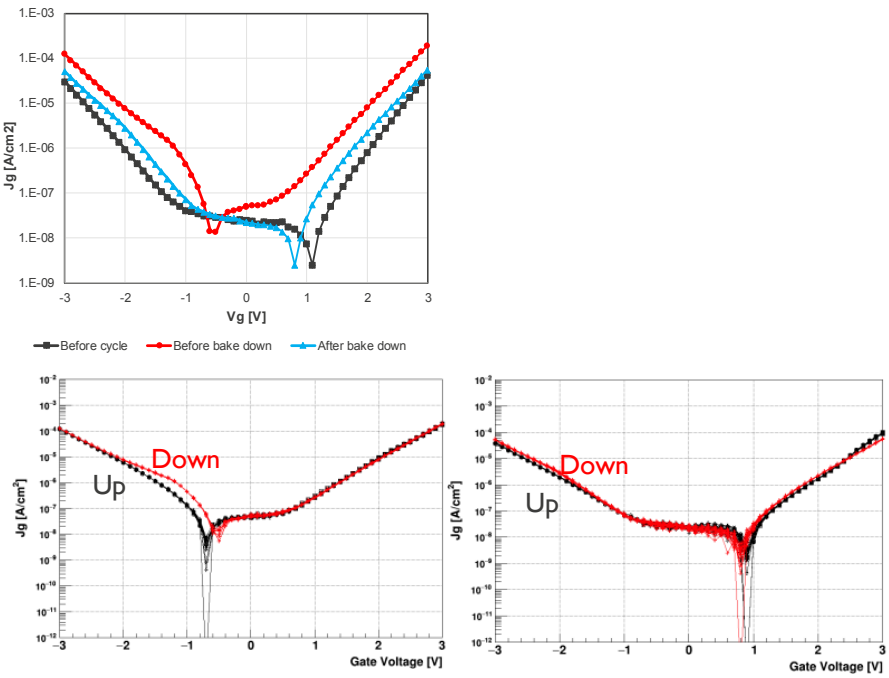


Figure 5 – (top) Comparison of I-V curves Before cycling, Before bake (=after cycling), and After bake; (bottom left) Before bake, after cycling ending with "Up" and "Down" states; and (bottom right) After bake, with cycling ending with "Up" and "Down" states.

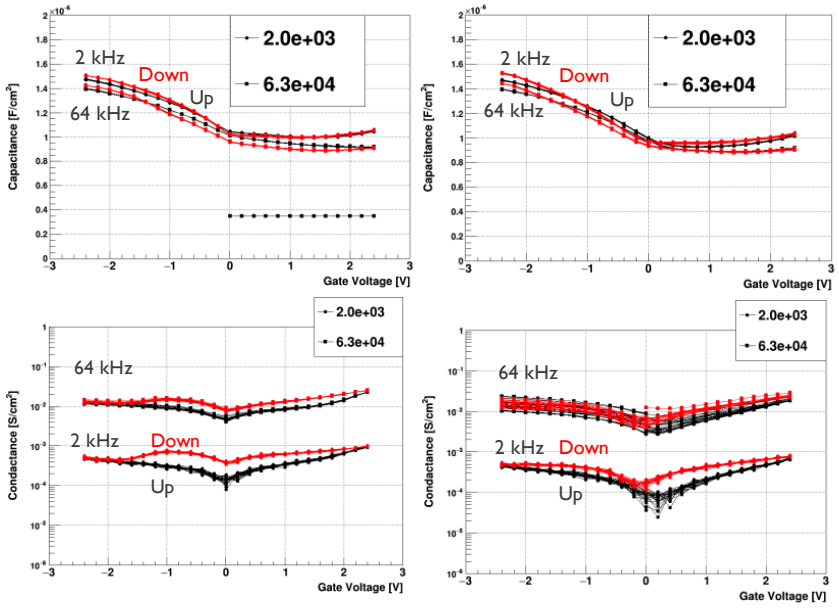


Figure 6 – Comparison of C-V (top row) and G-V (bottom row) characteristics at two frequencies (left) Before bake, after cycling ending with "Up" and "Down" states, and (right) After bake, with cycling ending with "Up" and "Down" states.

2.1.2 Ferroelectric Transistors

The FeFET devices were fabricated in the 28-nm SLP high-k/metal gate (HKMG) bulk process flow in a gate-first approach on 300 mm wafers by GLOBALFOUNDRIES in FAB1 in Dresden and measured by FMC unit, within this project.

The TiN/(doped[2])FE-HfO_2/SiO_2 layers deposited on top of the p-doped silicon substrate and capped with silicided polysilicon. The thickness of the ferroelectric HfO_2 layer is around 9 nm. Each 300 mm wafer was divided into 140 dies, each of which was patterned with GF MPW mask-set containing FeFET transistors and capacitors measured in this project. Switching, trapping and de-trapping experiments were performed on transistor with channel length (L) and width (W) of 450 nm and 450 nm, respectively. Gate leakage, gate capacitance and ferroelectric polarization measurements were performed on capacitor structures with channel length (L) and width (W) of 3000 nm and 3000 nm, respectively, multiplied by 50 and with shorted source and drain contacts. Pulsed I_D-V_G, Single Pulse I_D-V_G, polarization-voltage (P-V) measurements were carried out at 25°C and I_G-V_G was carried out at varying temperature.

The threshold voltage of the ferroelectric FET is variable, depending on the polarization of the ferroelectric layer. The memory effect relies upon reversible switching of the ferroelectric polarization. This polarization changes the conductivity of the silicon channel. Applying a negative gate voltage induces a switch of the polarization pointing towards the gate electrode. This corresponds to a lower channel conductivity and to a higher voltage threshold (HVT) for a FET with p- doped silicon substrate. On the other hand, applying a positive voltage reverses the polarization pointing towards the silicon channel, resulting in higher channel conductivity and lower voltage threshold (LVT). Figure 7 shows the pulsed drain current – gate voltage transfer characteristics of the HVT in blue and LVT in red after applying -4V 10us and +4V 10us, respectively to the gate for the complete 300mm wafer. The threshold voltage was extracted at a drain current of 1uA W/L. The threshold voltage difference between LVT and HVT is about 1.12 V on average, which is also the memory Window the FeFET. Moreover, the graph shows a normally distributed cumulative probability plot of the HVT and LVT. The memory window for all measured dies over the wafer is shown in Figure 8. It can be noted that the memory window shows a radial pattern and it is higher in the middle of the wafers.

The parameters for the pulsed I_D-V_G measurement are shown below. This I_D-V_G measurement and the corresponding V_{TH} extraction is used in the following to determine the threshold voltage shift for various switching, trapping and de-trapping experiment.

[2] The nature of the dopant species cannot be publicly disclosed due to confidentiality.

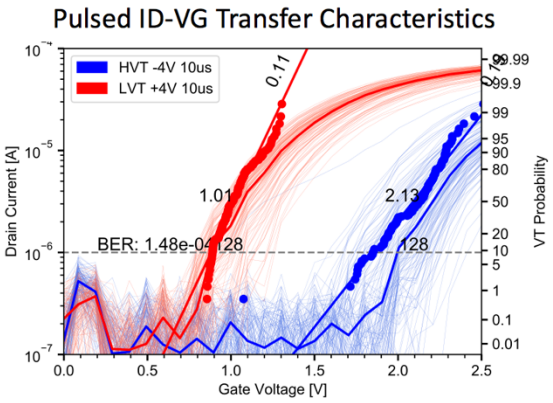


Figure 7 - I_D-V_G curves and cumulative probability plot of V_{TH} of the Device Under Test (DUTs) after applying a 10 bipolar wake-up cycles for different device geometries. Solid curves show the median I_D-V_G curve from 62 devices across wafer while solid lines show the fitting line of the probability plots.

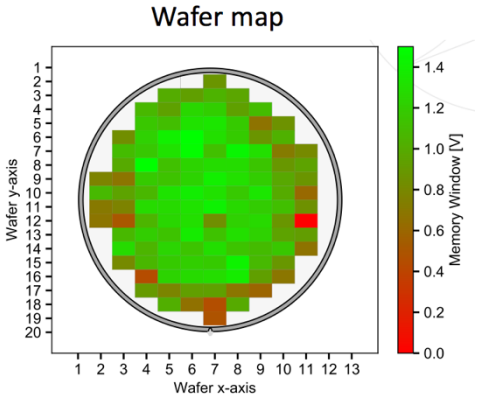


Figure 8 - Wafer map of MW after applying 10 bipolar wake-up cycles green color indicates larger MW while red color shows smaller MW.

Pulsed ID-VG:

- NI PXIe-5433 AWG, NI PXIe-5172 SCOPE, NplusT CFE
- V_G swept from 0 to +2.5 V (in 0.1V steps with 10 us per step duration), V_D was kept constant at 1V and V_S at 0V
- T = 25°C
- Devices with W=450 nm and L=450 nm

The LVT and HVT I_D-V_G measurement were executed after a 40 ms and 1 ms time delay after the write pulse, respectively. The criterion for choosing this specific time delay for the LVT and HVT measurement is based on the short-term retention test as shown in Figure 9 which reveals electron and hole de-trapping behavior. As it can be clearly seen in Figure 9, the device shows a strong electron de-trapping and hardly any hole de-trapping. The LVT states become stable after about 40 ms while the HVT states are already stable after 40 µs due to negligible hole trapping. Thus, a time delay of 40 ms and 1 ms after program and erase pulse are considered appropriate to read the V_{TH} by sweeping the gate voltage from 0 V to 2.5 V without being affected significantly by residual charge trapping. The desired behavior would be no electron or hole de-trapping to be able to directly read the threshold voltage after the write pulse of the LVT state. This trapping phenomena is linked to trap states in the FE-HfO_2. To better understand these trapping phenomena during the single pulse I_DV_G trapping experiments and simulation were performed.

The ferroelectric polarization reversal process itself is also highly time and voltage dependent. To better understand this time-voltage dependence, the switching voltage $V_{P,}$ for which the threshold voltage change is equal to half the maximum memory window for each cell, is extracted.

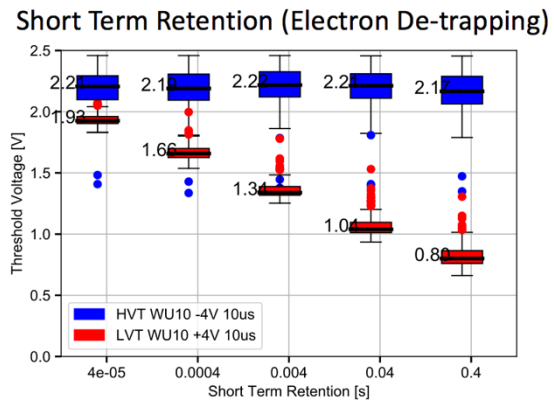


Figure 9 - Short term retention measurement of FeFETs with device geometry for HVT and LVT.

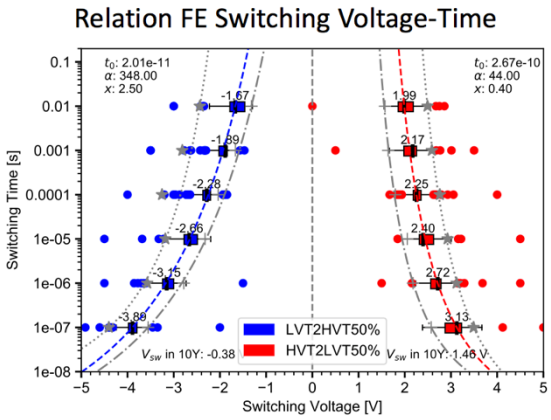


Figure 10 - Switching voltage V_S as a function of pulse width V_G for LVT to HVT (blue on the left panel) and HVT to LVT transition (red on the right panel). V_S is the pulse amplitude V_P for which the V_T change is half the full MW.

We indicate it with V_S, so that V_T (V_S) − *LVT* = 0.5 MW for the low- to high-V_{TH} transition and *HVT*− V_T (V_S) = 0.5 MW for the high- to low-V_T transition. Figure 10 shows t_S against the respective switching voltage amplitude V_p, where the left and right side of the axis correspond to the erase and program transitions, respectively. The experimental points clearly show an exponential dependence between t_S and V_G. This can be approximately described by

$$t_S = t_0 \, exp\left[\frac{\alpha}{(V_G - x)^2}\right], \quad (1)$$

where t_0, α and x describe the minimum switching time, exponential constant and voltage offset. This kind of switching dynamics has been explained by the classical nucleation theory applied to the ferroelectric polarization reversal.

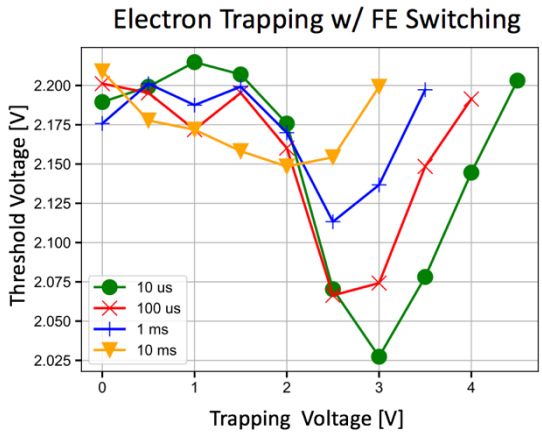


Figure 11 - LVT trapping and switching behavior of DUTs with 10 bipolar wake-up cycles and different pulse amplitudes shown for 4 different pulse widths. Reference polarization state for all pulse width and amplitudes is an HVT state written with -4V 10us.

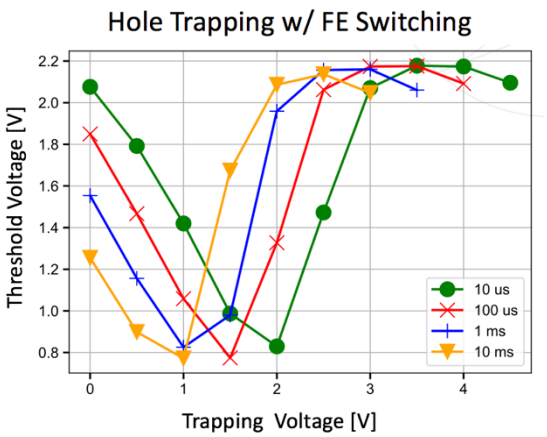
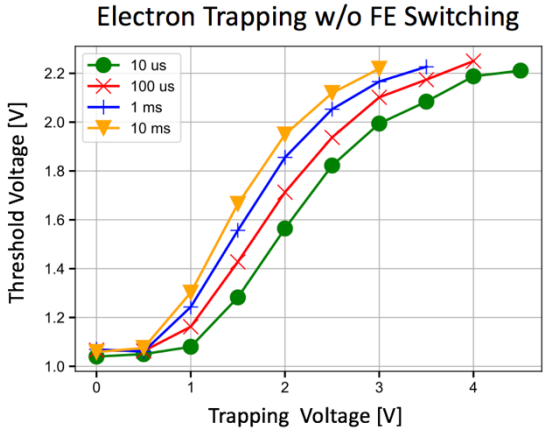


Figure 12 - HVT trapping and switching behavior of DUTs with 10 bipolar wake-up cycles and different pulse amplitudes shown for 4 different pulse widths. Reference polarization state for all pulse width and amplitudes is an HVT state written with -4V 10us.

In order to study the dependence of charge trapping and ferroelectric switching on the characteristics of FeFET devices experiments without delay time after the write pulse, for various pulse width, and amplitude were performed for various pulses in addition to the switching experiments in Figure 10. Figure 11 shows the LVT switching and trapping experiments. The reference state is an HVT erase with -4V 1us: it shows that no matter what pulse amplitude or width is chosen, the threshold voltage is close to the HVT state of about 2.1V. Since there is no wait time, the LVT and HVT state cannot be distinguished. Only after 40 ms as shown in Figure 9 the LVT becomes detectable by electron de-trapping. As for the HVT shown in Figure 12, the results of the same experiments become even more complicated. The reference state is in this case the trapped LVT state with a threshold voltage of 2.1V. By applying a negative voltage, the electrons are de-trapped first until the LVT with a threshold voltage of about 1V is reached. For longer pulse widths, such LVT is reached for lower pulse amplitudes. The polarization reversal to HVT starts for even more negative voltages only after this LVT is reached.

It is hence paramount to identify the trapping behavior of the ferroelectric HfO_2. Additional trapping experiments are implemented, such that after a write pulse (either program or erase) and after sufficient delay time, an additional pulse of same polarity compared to the write pulse but with variable amplitude is applied to the device. After this variable pulse amplitude, an immediate read-out is performed. Since the ferroelectric switching already occurred during the first write pulse, the trapping behavior can be independently measured for various pulse widths and amplitudes. Figure 13 and Figure 14 show that there is barely any hole trapping but a large amount of electrons trapping. Hole trapping shifts the HVT to lower voltages whereas electron trapping shifts the LVT to higher voltages. Since this represents the opposite direction compared to the effect of polarization switching on V_{TH}, charge injection leads to a MW decrease.



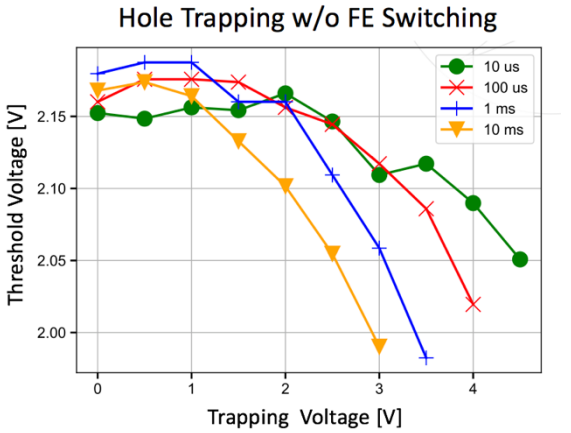


Figure 13 - LVT trapping behavior of DUTs with 10 bipolar wake-up cycles and different pulse amplitudes shown for 4 different pulse widths. Reference polarization state for all pulse width and amplitudes is a de-trapped LVT state (40ms wait time) programmed with +4V 10us.

Figure 14 - HVT trapping behavior of DUTs with 10 bipolar wake-up cycles and different pulse amplitudes shown for 4 different pulse widths. Reference polarization state for all pulse width and amplitudes is a de-trapped HVT state (1ms wait time) programmed with +4V 10us.

The experiments performed on the trapping behavior reveal the threshold voltage after the program pulse. In order to gain information about the threshold voltage during the program pulse, Single-pulse I_D-V_G measurements are used. The main advantage of this technique is the ability to capture the transient nature of the trapping processes. Time resolution in nanosecond time range can be provided. The stress pulse of certain amplitude and width is applied to the gate, while the drain current is simultaneously monitored (Figure 15 left). The drain current can be translated into I_D-V_G transfer characteristics for both rising and falling pulse edges (Figure 15 right). Basing on the threshold voltage shift extracted from these I_D-V_G transfer characteristics, conclusions about trapping/de-trapping behavior of the gate stack can be made. The main advantage of the single-pulse technique is that the time delay between stressing and sensing is eliminated; therefore the complete amount of trapped/de-trapped charges can be captured. Figure 15 shows the waveform applied to the FeFET gate. The FeFET is set to HVT by -4V 10us reference pulses. Afterwards, the drain current is measured on the rising and falling edge of the LVT pulse. During the hold time, the LVT pulse the devices switches and traps. As can be seen from the I_D-V_G measured, the threshold voltage can be up to 4V compared to 2V with standard pulsed I_D-V_Gs. This means that trapping is much more severe during the pulse, and this could influence the ferroelectric switching characteristics as well in a severe manner.

Single Pulse ID-VG:

- NI PXIe-5433 AWG, NI PXIe-5172 SCOPE, NplusT CFE
- V swept from 0 to pulse amplitude, pulse width time varied from 1us to 100ms, rising and falling edge slew rate 5us/1V, Drain voltage V_D = 0.1V and V_S =0.0V
- T = 25°C
  Devices with W=450 nm and L=450 nm

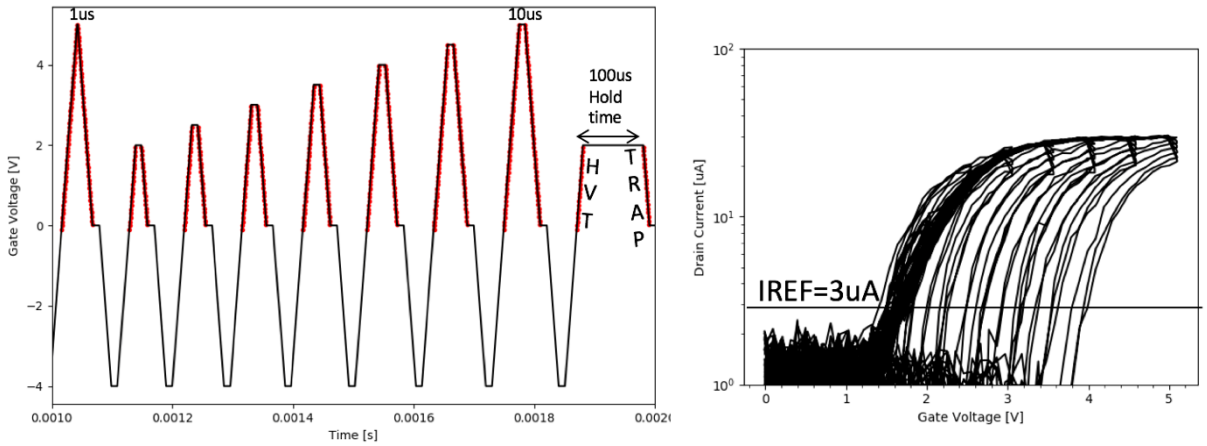


Figure 15 - Excerpt of the single-pulse waveform applied to the FeFET devices. Electron trapping can be identified either from the shift between I_DV_G transfer characteristics measured at the rising and falling edge of the LVT pulses.

It is important to compare the threshold voltage shift with the current flowing over the gate dielectric to extract a realistic trap distribution. Therefore, gate current – gate voltage I_G-V_G characteristics were measured with the following parameters.

I_G-V_G:

- NI PXIe-4135 HRSMU
- V swept from 0V to -4 V to 0V or from 0 to +4 V to 0V multiple times to avoid degradation and exclude ferroelectric switching events
- T = 25 – 125 C
- Devices with W=3000 nm and L=3000 nm multiplied by 50 and shorted Source/Drain

The waveform used to measure the gate leakage current is shown in Figure 16. First, a sweep to -4V and back was performed to bring the device in an HVT state. Another sweep to -4V and back to 0V was performed to measure the gate leakage without any switching contribution. The same procedure was performed for the LVT state. After the first measurement, the whole procedure was repeated to check that no degradation of the film occurred due to the measurement itself that would influence the trap extraction.

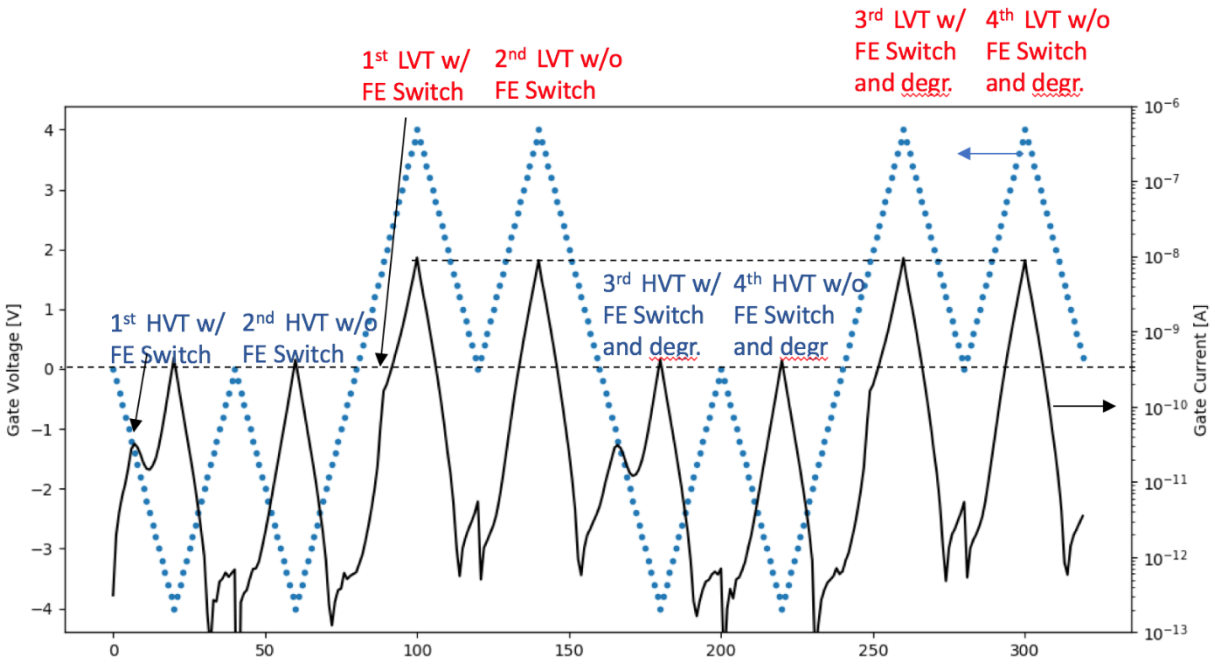


Figure 16 - Waveform used to measure the gate leakage current. Multiple sweeps are performed to distinguish the influence from FE switching and gate dielectric degradation.

The results plotted over gate voltage are shown in Figure 17 for two temperatures 25°C and 85°C. The contribution of FE switching to the gate current on the first up or down sweep can be clearly observed. Figure 18 shows the gate leakage current for temperatures ranging from 25°C to 125°C without any FE switching contribution.

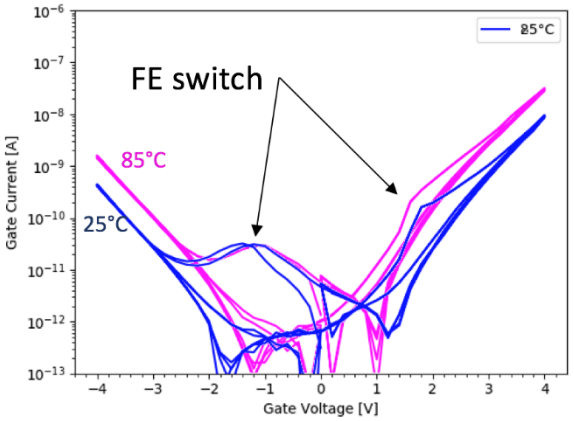


Figure 17 - Gate leakage current for 25°C and 85°C from the waveform shown in Figure 16.

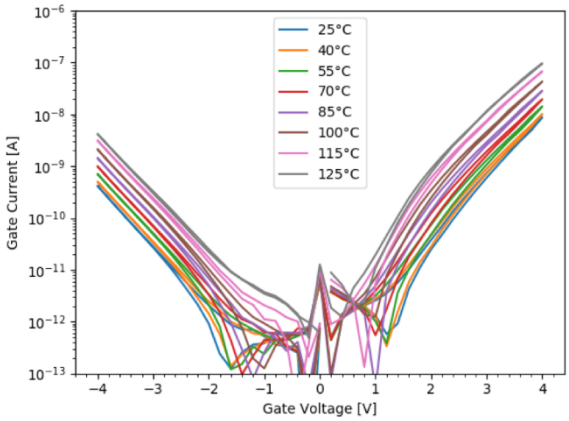


Figure 18 - Gate leakage current from 2nd HVT/LVT sweep in Figure 16 for multiple temperature ranging from 25°C-125°C.

2.2 The Defect Discovery Tool

The experimental data provided by IMEC and FMC units are fed into the Ginestra™ DDT with the aim of reproducing the voltage, frequency and temperature dependence of I-V and G-V characteristics to extract relevant material parameters and trap energy/space distribution. Figure 19 shows a schematic representation of the DDT workflow for the case of the leakage current measured on a single-layer MIM capacitor. It is comprised of few steps:

- Measured device/structure is re-created within the Ginestra™ simulation platform starting from the known device and material parameters (layers thickness, band-gap, dielectric constant, etc.).
- Measured experimental data are loaded into the DDT as in the case of the gate leakage currents as a function of the temperature shown on the left side of Figure 19.
- Device, material and – more importantly – trap parameters to be extracted (as well as their variation ranges) are selected from a dedicated panel of the DDT, see the central part of Fig. 19.
- Once the DDT is run, the selected parameters will be automatically varied within the specified intervals until the experimental data are accurately reproduced, (see the right part of Fig. 19). This process allows to extract the energy and space distribution of the traps as part of the results.

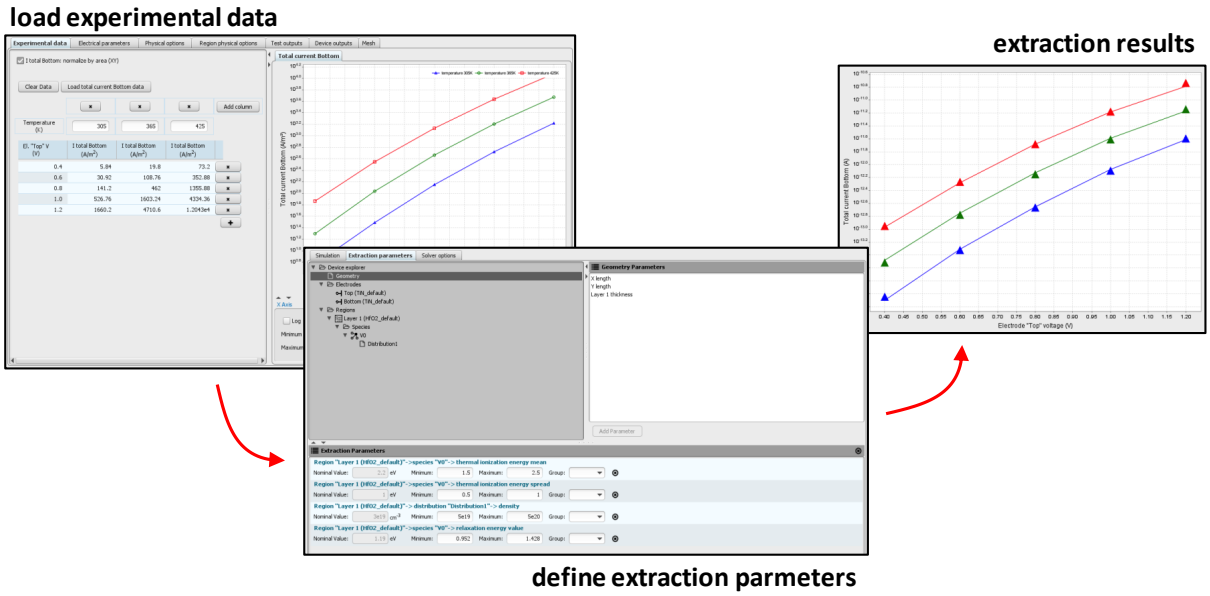


Figure 19 - I-V characteristics measured on multiple devices (top row) Before cycling (middle row) After cycling ending with Up and Down polarizations (measured after 1day at RT) (bottom row) After Baking (Up and Down polarizations).

2.3 Results and Discussion

The DDT-based methodology in the previous section is applied to the FE-HfO_2 samples described in Section 3.1.

Figure 20 shows the comparison between measured and simulated (with DDT) gate leakage currents as a function of the temperature on the SFS sample described in Section 3.1.1. An excellent agreement is obtained between experiments and simulations, and extracted material and trap parameters are reported in Table I.

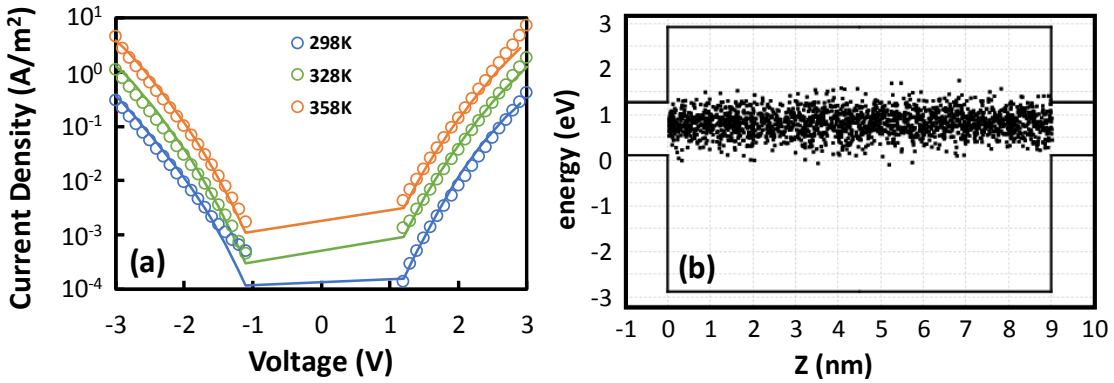


Figure 20 – (a) Current density simulated (lines) and measured (symbols) at different temperatures on Poly-Si/FE-HfO_2 (8 nm)/Si substrate capacitors described in Section 3.1.1. (b) Defect band extracted by applying DDT on the data in (a).

DDT results highlight the presence of a defect band located between ~1.6eV and ~2.5eV below HfO_2 conduction band bottom that well agrees with the energy levels reported in literature for positively charged oxygen vacancies [2], [3]. However, the extracted relaxation

energy [4], [2], that is directly connected to the atomic nature of the trap, is significantly larger, also with respect to the values reported for other possible vacancy states in pure HfO_2 (0.43eV, 0.48eV and 0.8eV for doubly negative, negative and neutral vacancies, respectively [5]). This clearly suggests the presence of a different trap state assisting the charge transport through Al-doped FE HfO_2 that will be investigated by means of DFT, also exploiting the interoperability of the IM2D box.

Table I – Trap parameters extracted using the DDT to reproduce I-V data measured as a function of temperature on the different FE devices.

	SFS devices	HKMG transistors	Literature [TED11],[EDL13]
Parameter	**Al-doped HfO_2**	**Si-doped HfO_2**	**HfO_2**
t_{IL} (nm)	-	0.7	-
t_{HfO2} (nm)	9	9.5	-
$N_{T,IL}$ (cm^{-3})	-	$2.28 \cdot 10^{19}$	-
$N_{T,HfO2}$ (cm^{-3})	$5 \cdot 10^{20}$	$1.5 \cdot 10^{20}$	10^{19} - $5 \cdot 10^{20}$
E_T (eV)	2.08	1.6	2.1
ΔE_T (eV)	0.8	0.2	1
E_{REL} (eV)	1.8	1.8	1.19

Figure 21 shows the comparison between measured and simulated (with DDT) threshold voltage shifts (ΔV_T) during fast constant voltage experiments performed at different gate voltages (see Figure 15 in Section 3.1.2). An excellent agreement is obtained in the whole range of voltages considered between experiments and simulations. Simulation results indicate the presence of a narrow defect band located at 1.6eV below HfO_2 conduction band bottom, as can be seen from the maps of the trapped charge extracted from the DDT simulations and reported in Figure 21. The ΔV_Ts are originated by defects located in the HfO_2 that trap the electrons injected because of the voltage applied to the gate during the experiment. A larger voltage leads to a larger amount of trapped charge.

Extracted material and trap parameters are reported in Table I. Similarly to the case of the Al-doped SFS devices, the defects in the doped-HfO_2 HKMG transistors are also characterized by a thermal ionization energies (E_T) that is within the range reported in the literature for positively charged oxygen vacancies [2], [3], whereas the extracted relaxation energy has the same higher value of 1.8eV. This again suggests the presence of a different trap state originating the observed threshold voltage shifts. Moreover, the same E_{REL} value found for the two different doped FE-HfO_2 films suggests a common nature of these traps, maybe related to the different structure of the HfO_2 material at the bases of the ferroelectricity.

Although the results obtained so far with DDT provide some interesting insights on the defects in FE-HfO_2, a more detailed analysis is needed to get comprehensive understanding and consistent explanation. This will be the focus of further activities within Tasks 3.1 and 3.3

of the project, where DDT will be applied to more data (see Section 3.1) and coupled with DFT calculations exploiting the IM2D box.

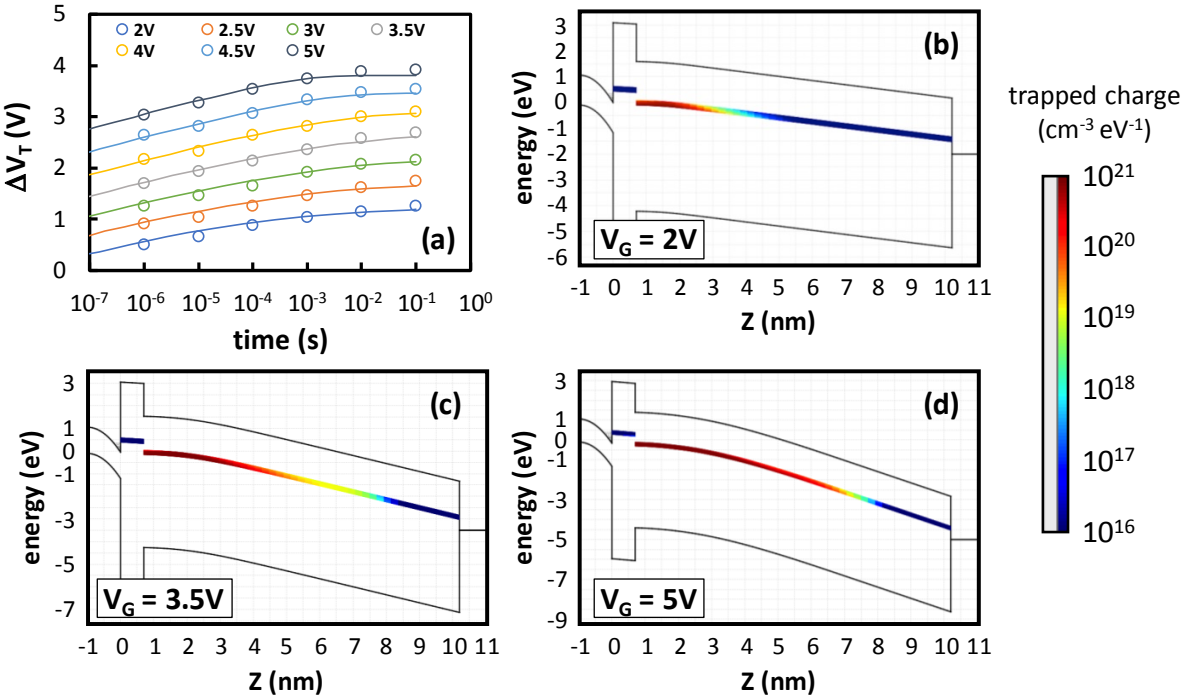


Figure 21 – (a) threshold voltage shifts simulated (lines) and measured (symbols) at different stress voltages on the HKMG transistors described in Section 3.1.2. (b)-(d) Defect band extracted by applying the DDT on the data in (a) when applying (b) 2V, (c) 3.5V and (d) 5V to the gate. The color scale indicates the amount of trapped charge.

ACRONYMS

ALD - Atomic Layer Deposition

DDT - Defect Discovery Tool

DFT - Density Functional Theory

DUT - Device Under Test

FE - Ferroelectric

HKMG - high-k/metal gate

HVT - Higher Voltage Threshold

IM2D - Interoperable Material-to-Device

LVT - Lower Voltage Threshold

MIM - Metal-Insulator-Metal

MW - Memory Window

SFS - Silicon-Ferroelectric-Silicon

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